Variable-Length Variable-Weight Prime Codes with Zero Cross Correlation for SAC-OCDMA Communication Systems

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Abstract: In this paper, a new code family called Variable-Length Variable-Weight (VLVW) prime code is presented for spectral-amplitude-coding optical code-division multiple-access (SAC-OCDMA) systems. These codes are constructed from the basic prime code groups. The code construction procedure is simple and the cross correlation value of the proposed new code is always zero. Thus it suppresses completely the phase-induced intensity noise and eliminates the effect of multi-user interference. Another important feature is that depending on the prime number (p), we can generate p numbers of code families each with different length and weight. Further, from the numerical analysis it is observed that the proposed code has better error performance and supports higher number of simultaneous users than the system with MQC codes and PMP codes. Also, the system with the proposed code supports approximately 230 number of simultaneous users for the given bit error rate (10^{-9}) when p=11, M=5 and w=11.

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1. Introduction

Optical code-division multiple-access (OCDMA) is a spread spectrum [1,2] technology and it has several features like asynchronous access capability, provision for adding more users, security, simplified network control, protection against jamming and possibility of multimedia traffic. Since OCDMA is a spread spectrum system, multiple users share a single bandwidth transmission channel. Thus, this property introduces interference in the system called multi-user interference. Presence of MUI degrades the system performance and can be eliminated or completely suppressed by the suitable encoder and decoder structure which in turn depends on the codes used in it.

Depending on the detection mechanisms used, OCDMA system is classified into incoherent OCDMA system and coherent OCDMA system. Compared to incoherent, coherent systems require complex circuits and become expensive. In addition conventional OCDMA systems are divided into synchronous and asynchronous systems based on the time synchronization technique. Modified prime codes and optical orthogonal codes are commonly used as the spreading codes respectively for the above said types. Further, according to the spreading technique supported by the system, OCDMA system is categorized into temporal-amplitude-coding and spectral-amplitude-coding (SAC) OCDMA systems. In this work incoherent synchronous spectral-amplitude-coding OCDMA system is considered for our analysis.

The performance of SAC OCDMA system mainly depends on the auto and cross correlation properties of the signature sequences used in the encoder and decoder circuits. In addition with MUI effect, due to spontaneous emission SAC OCDMA system introduces the phase-induced intensity-noise (PIIN). These two major drawbacks can be overcome by using the signature codes with low and constant in-phase cross-correlation (IPCC) values. So far many numbers of codes have been proposed in the literature for SAC OCDMA systems. Signature code development procedure depends on the IPCC value of the code [3-7], code length [8-11] and code weight [12-14] of the code family. All these proposed code families have the limitations in one way or another. Recently a new code called ZCC is proposed in [15]. The disadvantage of this code is that longer code length and it requires higher number of mapping steps in order to achieve the particular code size for the given w. Therefore, in this paper a new code group family named variable-length variable-weight (VLVW) code is proposed. The code is developed from the basic prime code sequences. The important feature of the code is that cross correlation value of the proposed code is always zero irrespective of the code length and code weight values. Thus, the system with the proposed code supports different code families each with higher number of simultaneous users and with low bit error rate performance.

2. Code Construction

The proposed VLVW codes are derived from the basic prime code group. The basic prime codes are the set of prime code sequences. These prime code sequences can be generated from the Galois field GF(p) = {0,1, . . . , p-1}, p represents the number of prime sequences. The various steps needed to construct the VLVW code family is given below.

Step 1:

For example, consider the code construction procedure for p=5 VLVW code family.

Since the proposed codes are the family of basic prime codes, first generate the basic prime sequences using the Galois field for p=5. The prime code sequences for p=5 is shown in Table 1.

Table 1 Prime code sequences

.	0	1	2	3	4
0	0	0	0	0	0
1	0	1	2	3	4
2	0	2	4	1	3
3	0	3	1	4	2
4	0	4	3	2	1

Normally the prime code sequences from the table are represented by 00000, 01234, 02413, 03142 and 04321.

But, in this case in order to have the codes with different weights, the diagonal elements are considered as the prime sequences. Since the upper and lower diagonal elements are same, the prime sequences are represented by 0, 04, 033, 0212 and 01441.

Step 2:

Consider the generated prime sequences be the source sequence for the different code sequence families. For p=5 there are five source sequences. From these five source sequences, we can generate five code families with different code weight. The code families with their source sequences are given by

$PC_{w=1} = [0]$

$PC_{w=2} = [0\ 4]$

$PC_{w=3} = [0\ 3\ 3]$

$PC_{w=4} = [0\ 2\ 1\ 2]$

$PC_{w=5} = [0\ 1\ 4\ 4\ 1]$. Here, $PC_{w=1}$, $PC_{w=2}$, . . . represents different code families with code weight w=1, w=2, . . .

In general, from 'p' prime numbers we can generate 'p' numbers of code families with weight w=1, w=2, . . . , w=p.

Step 3:

From the source sequence of each group, generate a set of sequences by time shifting the individual prime number present in the source sequence by one unit.

$$PC_{w=1} = \begin{bmatrix} 0 \\ 1 \\ 2 \\ 3 \\ 4 \end{bmatrix}$$

$$PC_{w=2} = \begin{bmatrix} 0 & 4 \\ 1 & 0 \\ 2 & 1 \\ 3 & 2 \\ 4 & 3 \end{bmatrix}$$

$$PC_{w=3} = \begin{bmatrix} 0 & 3 & 3 \\ 1 & 4 & 4 \\ 2 & 0 & 0 \\ 3 & 1 & 1 \\ 4 & 2 & 2 \end{bmatrix}$$

$$PC_{w=4} = \begin{bmatrix} 0 & 2 & 1 & 2 \\ 1 & 3 & 2 & 3 \\ 2 & 4 & 3 & 4 \\ 3 & 0 & 4 & 0 \\ 4 & 1 & 0 & 1 \end{bmatrix}$$

$$PC_{w=5} = \begin{bmatrix} 0 & 1 & 4 & 4 & 1 \\ 1 & 2 & 0 & 0 & 2 \\ 2 & 3 & 1 & 1 & 3 \\ 3 & 4 & 2 & 2 & 4 \\ 4 & 0 & 3 & 3 & 0 \end{bmatrix}$$

Now, each code family supports five code sequences. Generally, after the completion of time shifting each code family supports 'p' number of code sequences.

Step 4:

In order to further increase the number of code sequences supported by the system, a mapping technique is used.

For $PC_{w=1}$ code family,

$$PC_{w=1,\ M=1} = \begin{bmatrix} X & 0 \\ X & 1 \\ X & 2 \\ X & 3 \\ X & 4 \\ 0 & X \\ 1 & X \\ 2 & X \\ 3 & X \\ 4 & X \end{bmatrix}$$

$$PC_{w=1,\ M=2} = \begin{bmatrix} X & X & X & 0 \\ X & X & X & 1 \\ X & X & X & 2 \\ X & X & X & 3 \\ X & X & X & 4 \\ X & X & 0 & X \\ X & X & 1 & X \\ X & X & 2 & X \\ X & X & 3 & X \\ X & X & 4 & X \\ X & 0 & X & X \\ X & 1 & X & X \\ X & 2 & X & X \\ X & 3 & X & X \\ X & 4 & X & X \\ 0 & X & X & X \\ 1 & X & X & X \\ 2 & X & X & X \\ 3 & X & X & X \\ 4 & X & X & X \end{bmatrix}$$

In general

$$PC_{w=1,M} = \begin{bmatrix} X & PC_{w=1,M-1} \\ PC_{w=1,M-1} & X \end{bmatrix}$$

here, X = null with ‘p’ numbers of zeros.
For $PC_{w=2}$ code family,

$$PC_{w=2,\ M=1} = \begin{bmatrix} X & X & 0 & 4 \\ X & X & 1 & 0 \\ X & X & 2 & 1 \\ X & X & 3 & 2 \\ X & X & 4 & 3 \\ 0 & 4 & X & X \\ 1 & 0 & X & X \\ 2 & 1 & X & X \\ 3 & 2 & X & X \\ 4 & 3 & X & X \end{bmatrix}$$

In general

$$PC_{w=2,M} = \begin{bmatrix} X & PC_{w=2,M-1} \\ PC_{w=2,M-1} & X \end{bmatrix}$$

For $PC_{w=3}$ code family,

$$PC_{w=3,\ M=1} = \begin{bmatrix} X & X & X & 0 & 3 & 3 \\ X & X & X & 1 & 4 & 4 \\ X & X & X & 2 & 0 & 0 \\ X & X & X & 3 & 1 & 1 \\ X & X & X & 4 & 2 & 2 \\ 0 & 3 & 3 & X & X & X \\ 1 & 4 & 4 & X & X & X \\ 2 & 0 & 0 & X & X & X \\ 3 & 1 & 1 & X & X & X \\ 4 & 2 & 2 & X & X & X \end{bmatrix}$$

In general

$$PC_{w=3,M} = \begin{bmatrix} X & PC_{w=3,M-1} \\ PC_{w=3,M-1} & X \end{bmatrix}$$

For $PC_{w=4}$ code family,

$$PC_{w=4,\ M=1} = \begin{bmatrix} X & X & X & X & 0 & 2 & 1 & 2 \\ X & X & X & X & 1 & 3 & 2 & 3 \\ X & X & X & X & 2 & 4 & 3 & 4 \\ X & X & X & X & 3 & 0 & 4 & 0 \\ X & X & X & X & 4 & 1 & 0 & 1 \\ 0 & 2 & 1 & 2 & X & X & X & X \\ 1 & 3 & 2 & 3 & X & X & X & X \\ 2 & 4 & 3 & 4 & X & X & X & X \\ 3 & 0 & 4 & 0 & X & X & X & X \\ 4 & 1 & 0 & 1 & X & X & X & X \end{bmatrix}$$

In general

$$PC_{w=4,M} = \begin{bmatrix} X & PC_{w=4,M-1} \\ PC_{w=4,M-1} & X \end{bmatrix}$$

For $PC_{w=5}$ code family,

$$PC_{w=5,\ M=1} = \begin{bmatrix} X & X & X & X & X & 0 & 1 & 4 & 4 & 1 \\ X & X & X & X & X & 1 & 2 & 0 & 0 & 2 \\ X & X & X & X & X & 2 & 3 & 1 & 1 & 3 \\ X & X & X & X & X & 3 & 4 & 2 & 2 & 4 \\ X & X & X & X & X & 4 & 0 & 3 & 3 & 0 \\ 0 & 1 & 4 & 4 & 1 & X & X & X & X & X \\ 1 & 2 & 0 & 0 & 2 & X & X & X & X & X \\ 2 & 3 & 1 & 1 & 3 & X & X & X & X & X \\ 3 & 4 & 2 & 2 & 4 & X & X & X & X & X \\ 4 & 0 & 3 & 3 & 0 & X & X & X & X & X \end{bmatrix}$$

In general

$$PC_{w=5,M} = \begin{bmatrix} X & PC_{w=5,M-1} \\ PC_{w=5,M-1} & X \end{bmatrix}$$

Thus, by increasing the mapping steps (M) we can increase the number of codes.

Step 5:

The above said code family contains X and the numbers 0,1,2,3 and 4. In general the code sequences may contain X, 0, 1, 2, . . . , p-1. Therefore, the variable-length variable-weight prime codes can be represented by placing ‘1’ at the p^{th} position with p-1 zeros.

VLVW prime code for $PC_{w=1}$:

$$VLVW_{w=1,\ M=1} = \begin{bmatrix} 00000 & 10000 \\ 00000 & 01000 \\ 00000 & 00100 \\ 00000 & 00010 \\ 00000 & 00001 \\ 10000 & 00000 \\ 01000 & 00000 \\ 00100 & 00000 \\ 00010 & 00000 \\ 00001 & 00000 \end{bmatrix}$$

$$VLVW_{w=1,\ M=2} = \begin{bmatrix} 00000 & 00000 & 00000 & 10000 \\ 00000 & 00000 & 00000 & 01000 \\ 00000 & 00000 & 00000 & 00100 \\ 00000 & 00000 & 00000 & 00010 \\ 00000 & 00000 & 00000 & 00001 \\ 00000 & 00000 & 10000 & 00000 \\ 00000 & 00000 & 01000 & 00000 \\ 00000 & 00000 & 00100 & 00000 \\ 00000 & 00000 & 00010 & 00000 \\ 00000 & 00000 & 00001 & 00000 \\ 00000 & 10000 & 00000 & 00000 \\ 00000 & 01000 & 00000 & 00000 \\ 00000 & 00100 & 00000 & 00000 \\ 00000 & 00010 & 00000 & 00000 \\ 00000 & 00001 & 00000 & 00000 \\ 10000 & 00000 & 00000 & 00000 \\ 01000 & 00000 & 00000 & 00000 \\ 00100 & 00000 & 00000 & 00000 \\ 00010 & 00000 & 00000 & 00000 \\ 00001 & 00000 & 00000 & 00000 \end{bmatrix}$$

VLVW prime code for $PC_{w=2}$:

$$VLVW_{w=2,\ M=1} = \begin{bmatrix} 00000 & 00000 & 10000 & 00001 \\ 00000 & 00000 & 01000 & 10000 \\ 00000 & 00000 & 00100 & 01000 \\ 00000 & 00000 & 00010 & 00100 \\ 00000 & 00000 & 00001 & 00010 \\ 10000 & 00001 & 00000 & 00000 \\ 01000 & 10000 & 00000 & 00000 \\ 00100 & 01000 & 00000 & 00000 \\ 00010 & 00100 & 00000 & 00000 \\ 00001 & 00010 & 00000 & 00000 \end{bmatrix}$$

VLVW prime code for $PC_{w=3}$ code family:

$$VLVW_{w=3,\ M=1} = \begin{bmatrix} 00000 & 00000 & 00000 & 10000 & 00010 & 00010 \\ 00000 & 00000 & 00000 & 01000 & 00001 & 00001 \\ 00000 & 00000 & 00000 & 00100 & 10000 & 10000 \\ 00000 & 00000 & 00000 & 00010 & 01000 & 01000 \\ 00000 & 00000 & 00000 & 00001 & 00100 & 00100 \\ 10000 & 00010 & 00010 & 00000 & 00000 & 00000 \\ 01000 & 00001 & 00001 & 00000 & 00000 & 00000 \\ 00100 & 10000 & 10000 & 00000 & 00000 & 00000 \\ 00010 & 01000 & 01000 & 00000 & 00000 & 00000 \\ 00001 & 00100 & 00100 & 00000 & 00000 & 00000 \end{bmatrix}$$

VLVW prime code for $PC_{w=4}$ code family:

$$VLVW_{w=4,\ M=1} = \begin{bmatrix} 00000 & 00000 & 00000 & 00000 & 10000 & 00100 & 01000 & 00100 \\ 00000 & 00000 & 00000 & 00000 & 01000 & 00010 & 00100 & 00010 \\ 00000 & 00000 & 00000 & 00000 & 00100 & 00001 & 00010 & 00001 \\ 00000 & 00000 & 00000 & 00000 & 00010 & 10000 & 00001 & 10000 \\ 00000 & 00000 & 00000 & 00000 & 00001 & 01000 & 10000 & 01000 \\ 10000 & 00100 & 01000 & 00100 & 00000 & 00000 & 00000 & 00000 \\ 01000 & 00010 & 00100 & 00010 & 00000 & 00000 & 00000 & 00000 \\ 00100 & 00001 & 00010 & 00001 & 00000 & 00000 & 00000 & 00000 \\ 00010 & 10000 & 00001 & 10000 & 00000 & 00000 & 00000 & 00000 \\ 00001 & 01000 & 10000 & 01000 & 00000 & 00000 & 00000 & 00000 \end{bmatrix}$$

In the above code set number of rows represents code size (simultaneous users K), columns represents code length (N). The cross correlation value of the code families is always zero independent of the code weight and code length. The relationship between code size and code length of the individual code family is given below.

For $PC_{w=1}$ code family

When w=1, M=0; K=5, N=5

w=1, M=1; K=10, N=10, etc.,

For $PC_{w=2}$ code family

When w=2, M=0; K=5, N=10

w=2, M=1; K=10, N=20, etc.,

For $PC_{w=3}$ code family

When w=3, M=0; K=5, N=15

w=3, M=1; K=10, N=30, etc.,

For $PC_{w=4}$ code family

When w=4, M=0; K=5, N=20

w=4, M=1; K=10, N=40, etc.,

For $PC_{w=5}$ code family

When w=5, M=0; K=5, N=25

w=5, M=1; K=10, N=50, etc.,

Hence, increasing the mapping steps increases the number of simultaneous users. The mathematical relationship between K and N can be generalized into

$$K=2^M * p \qquad (1)$$

$$N=2^M * w * p. \qquad (2)$$

Where M represents number of mappings, p – prime number, w –weight

3. Performance Analysis

Generally, SAC OCDMA system performance depends on phase-induced intensity noise, shot noise and thermal noise. But in the proposed work, since the cross correlation value is always zero, the bit error rate performance is analyzed by considering only shot noise and thermal noise. That is, it is assumed that the effects of PIIN are neglected.

An expression for the SNR and BER performance of the SAC OCDMA system can be represented by

$$SNR = \frac{\frac{R^2 P_{sr}^2 w^2}{N^2}}{2eBP_{sr}R\frac{wK}{N} + \frac{4K_B T_n B}{R_L}} \qquad (3)$$

Where the terms in the denominator represents shot noise and thermal noise. Here, R is the responsivity of the photodiode and is given by R = (ηe)/(hf_c), where h is the plank's constant (6.626x10^{-34}), f_c is the frequency of the broad band optical pulse in Hz, η is the quantum efficiency (0.6), e is the electronic charge (1.602x10^{-19}), P_s is the effective source power at the receiver in watts, K_B is Boltzmann's constant(1.379x10^{-23}), R_L is the Load resistance in ohms 1030Ω and T_n is Absolute Temperature in degrees Kelvin 300K. It is also assumed that emission wavelength of the broadband source as 1.55μm. The bit error rate (BER) performance of the system can be calculated from signal to noise ratio using

$$BER = \frac{1}{2}\operatorname{erfc}\sqrt{\frac{SNR}{8}} \qquad (4)$$

Where erfc - A complementary error function

4. Results and Discussion

The bit error rate performance of the SAC OCDMA system with the proposed code for p=11, M=5 (M may take any value), w = 2, 5, 8 and 11 is shown in figure 1. From p=11, we can generate 11 code families with weight w = 1, 2, 3, . . . , 11. The graph is drawn only for w = 2, 5, 8 and 11. The system supports 11 code families each with 352 (K = 2^M p) number of simultaneous subscribers and the code length (N=2^M pw) of the system varies depending on the code weight. The proposed system performance is compared to the system with the commonly used MQC code for p=11. MQC code supports only one set of 121 simultaneous users with weight w = 12 and the code length of the system is 132. From figure 1, it is observed that the proposed system has much better performance even with w =2 than the system with MQC codes. Also, it is observed that the system with the proposed code supports approximately 230 number of simultaneous users for the given bit error rate (10^{-9}) but MQC supports only approximately 48 users.

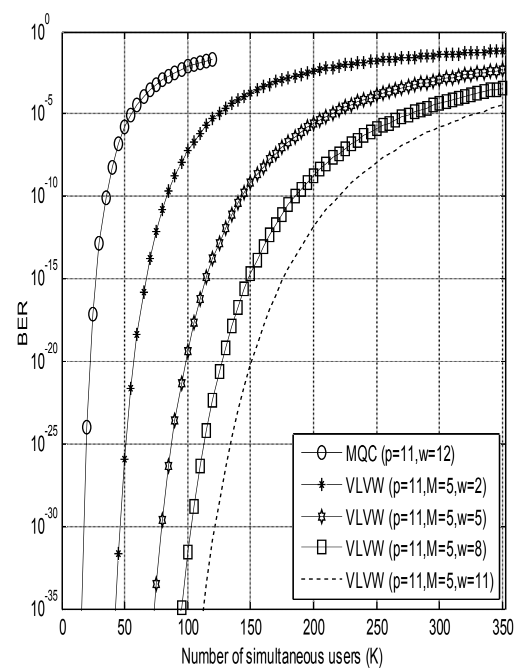

Figure 1. The number of simultaneous users versus the BER for p=11 at the effective source power equal to -10dBm.

Figure 2. illustrates the BER performance of the proposed code with the PMP code for p =11. The code size of the proposed code for p = 11 and M = 6 is 704 that is the proposed code supports 11 code families each with 704 number of simultaneous users whereas the PMP code supports only two code families with either 242 or 605 (K = Mp^2) number of simultaneous subscribers. Further, PMP supports only 2 types of code weight (w = (p-1) / M, where M is the factor of p), but our proposed code supports 11 types of code weight. Figure 2 reveals that the performance of the proposed code is much better compared to the PMP codes. Also, it is observed that increase in the code weight improves the performance of the system and the number of simultaneous users supported for the given bit error rate (10^{-9}).

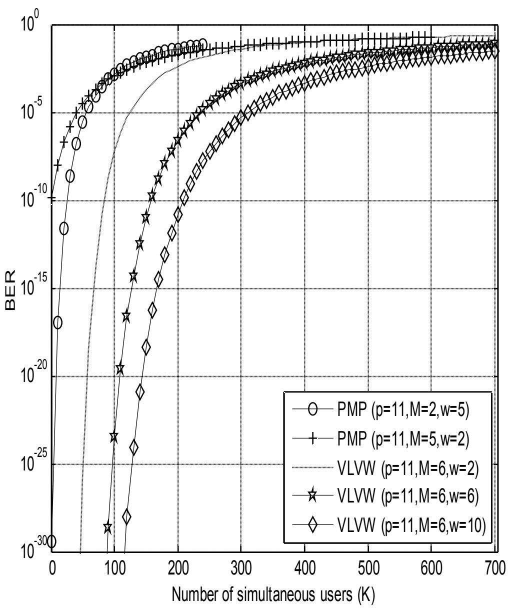

Figure 2. The number of simultaneous users versus the BER for p=11 at the effective sourcepower equal to -10dBm.

Table 2 . shows comparison of performance parameters in ZCC and VLVW code families.

Table 2 Comparison between ZCC and VLVW prime code family

Type of code family	No.of users (K)	Codeweight (w)	Codelength (N)
ZCC	2^m (w+1)	w = 1,2 ,3, …	2^m w (w+1)
VLVW prime code	2^M p	w = 1,2, 3,…p	2^M w p

From the theoretical comparison, it is observed that code size of VLVW and ZCC code depends on p, M and m, w respectively. For the given prime number p and M, the number of simultaneous users supported by the system with VLVW code is greater compared to the system with ZCC code (if p = 17, M = m =4 and w = 11 then K (VLVW) = 272 and K (ZCC) = 192).

5 . Conclusion

In this paper, we have proposed a family of prime codes called Variable-Length Variable-Weight prime code mainly to suppress the effect of phase induced intensity noise and to increase the number of simultaneous users supported by the SAC OCDMA system. These codes are derived from the basic prime codes and using this simple procedure, we can generate the code families starting from the code family with weight 1 to code family with weight p. Since the cross correlation value of this code family is always zero, the proposed code family effectively suppresses the phase induced intensity noise and thus improves the system performance. Further, the system supports higher number of simultaneous users because the code size of the code depends on the value of M. Finally, from the theoretical analysis it is observed that the bit error performance of the proposed code is much better compared with MQC codes and PMP codes. In addition it supports greater number of users compared to the system with ZCC code.

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