A Design of Fault Tolerant Reversible Arithmetic Logic Unit

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Abstract: Since the Arithmetic Logic Unit (ALU) is one of the essential components of the Central Processing Unit (CPU), its well performance is the most important factor in obtaining the high reliability. The reversible logic has also found emerging attention in nanotechnology, optical computing, quantum computing and low power CMOS design. In this paper we are going to propose and analyze a basic model of fault tolerant reversible ALU and show that the realization of an efficient fault tolerant reversible ALU is possible with both minimum constant inputs and garbage outputs. The proposed fault tolerant reversible ALU is a versatile approach to the implementation of quantum computing with having both a remarkable low power consumption and nano scaling.
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Introduction

This paper proposes an efficient fault tolerant reversible arithmetic logic unit. Traditional irreversible hardware computation inherently leads to the energy losses due to the missing bit information, where the energy dissipation is proportional to the number of missing bits [1]. Bennet showed that to avoid this energy loss in a logic circuit is to use reversible logic gates [2]. A gate is reversible if there is a one-to-one mapping of the input/output. That is the relationship between input/output has to be an injective one. For this main reason, reversible logic has received significant attention and proven to have applications in areas such as optical computing, low power electronic design, DNA, quantum computing, and nanotechnology based systems to name a few [3],[4],[5]. It should be noted that the non existence of both any fan out and feed back (loop) are two major problems with the reversible logic synthesis. Thus, the synthesis and implementation of the reversible logic circuit becomes more complex than the conventional one [4], [5]

If a system is made up of fault tolerant components, then it will be able to continue operating properly when the failure occurs in some of its components. The detection and correction of faults in such fault tolerant systems are easier. We can achieve fault tolerance in many systems by using parity bits. Thus, parity preserving reversible circuit design will be very important for development of fault tolerant reversible systems in nanotechnology which is an emerging technology [6]. It is worth to note that the parity preserving gates can be used to make fault tolerant reversible logic circuits.

2. Novel Design

2.1. Reversible, Quantum Gates and Circuits

A gate, a circuit or a function is reversible if and only if there is a one-to-one mapping between its input and output. Therefore, a reversible gate has an equal number of inputs and outputs. There is a number of commonly used reversible logic gate such as Feynman Gate, FG [7], Toffoli Gate, TG [8] and Peres Gate, PG [9].

A 2×2 Feynman Gate, also known as controlled NOT (1-CNOT), is depicted in Fig.1a. The 3×3 reversible Peres and Toffoli gates are also shown in Fig. 1b and Fig 1.c, respectively with both of them being universal gates. On the other hand consider a 3*3 Toffoli gate, we know that the two of the inputs are mapped to the first two outputs and if both of the first inputs are one then the result will be complemented, otherwise the third output will be the same as the third input.

Peres gate (PG), is equivalent to the transformation produced by a Toffoli gate followed by a Feynman gate. The Feynman gate and the Peres gate are one-through gates, (i.e. one of the input lines is also output). The Toffoli gate is two-through gate, that is two of the input lines are also outputs.

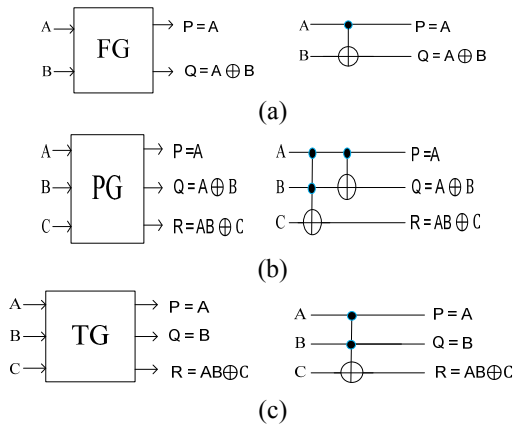


Fig. 1: commonly used reversible logic gates. a) Feynman gate; b) Peres gate; c) Tofolli gate

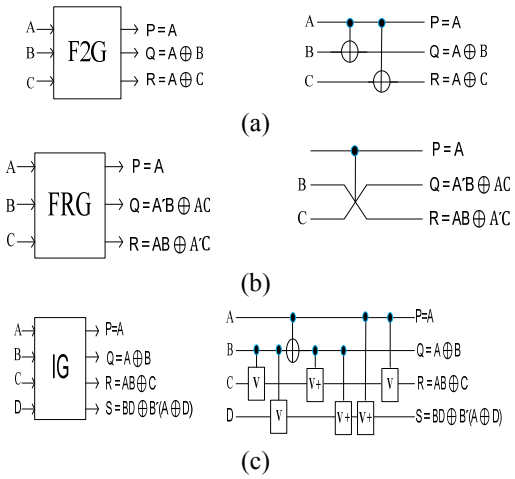
2.2. Parity Preserving Reversible Gates and Circuits

Between reversible logic gates, those with their input parity being the same as their output parity are called "parity preserving reversible gates (circuits)". Most of arithmetic and other processing functions do not preserve the parity of the data. Parity checking is one of the most widely used methods for error detection in digital logic systems [12], [13], [14]. Therefore it is important to construct parity preserving reversible gates and circuits. There are some problems using standard methods of error detection in reversible circuits, since fan-out is not allowed, and it may increase the number of gates being used along with the number of garbage outputs being produced. Given that reversible logic gates have the equal number of inputs and outputs, a sufficient requirement for parity preservation of a reversible circuit is that each gate to have a parity-preserving characteristics. Thus, a sufficient condition for having a parity preserving reversible logic gates is the implementation of the reversible circuit with each gate being parity preserving. In figure 2, three different parity preserving reversible gates along with truth table is shown [6], [12], [15].

3. The proposed Fault Tolerant Reversible Arithmetic Logic Unit

An ALU unit is a multi-functional circuit that conditionally performs one of several possible functions on two operands say, A and B, depending on a control unit. Mathematician John Von Neumann proposed the ALU concept in 1945, where he laid the foundations for a new computer called the "EDVAC" [16]. Knowing that ALU performs all arithmetic logic operations, it is considered to be the fundamental building block of the central processing unit (CPU).

In general there are two design considerations for serial and parallel ALU with reversible circuits [17].To optimize the speed and cost we have used a fault tolerant reversible ALU with combinations of both parallel and serial structures. To implement any one of four basic logical operations, AND, OR, EX-OR and ADD a reversible fault tolerant 4×1 multiplexer along with three FRG gates which is expandable to $2^n \times 1$ and shown in figure 3 , is used. The important property of this circuit structure is that by using a fault tolerant full adder(FTFA) block for computations of EX-OR and ADD the gate number and the quantum cost both are decreased by a factor of one. In figure 4, the two different design representations are also shown.



A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	1
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	0	0

(d)

Fig 2: a) Feynman Double gate; b) Fredkin Gate; c) IG Gate; d) the FRG truth table.

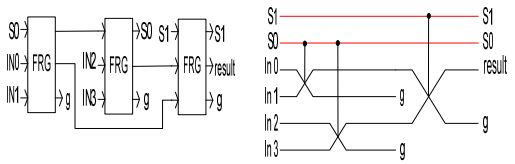
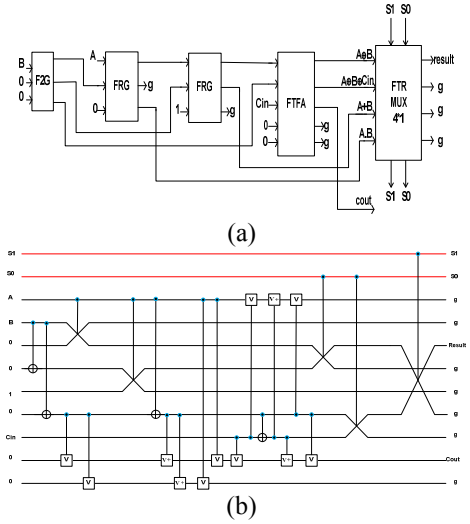


Fig. 3: proposed fault tolerant reversible 4×1 multiplexer.



(a)

(b)

Fig 4: a) fault tolerant reversible ALU with fault tolerant reversible gates.
b) Equivalent quantum representation of fault tolerant reversible ALU.

Before doing any type of computation we define the constant input as being zero or one, the garbage output being the one which is not used for further computations , and the quantum cost is considered to be as the number of reversible logic gates which are either 1×1 or 2×2 reversible.

With the four main factors of circuit complexity defind as:

α = A two input EX-OR gate calculation
β = A two input AND gate calculation
δ = A NOT calculation
T = Total logical calculation

The table 2 shows the result of the computations for n×1 multiplexer and n-bit ALU:

Table 2

	Constant Input	Garbage Output	Total Number of Gates	Quantum Cost	Total Logic Calculation
Fault tolerant reversible multiplexer $2^n * 1$	$0^{\dagger}$	$2^n - 1$	$2^n - 1$	$10^n - 5$	$(2^n - 1) \times (2\alpha + 4\beta + 2\delta)$
Fault tolerant reversible ALU(nbit)	6n	7n	7n	41n	$n \times (20\alpha + 26\beta + 12\delta)$

†: Optimum value

4. Conclusion

We have shown that a fault tolerant reversible basic arithmetic logic unit and a fault tolerant reversible 4×1 multiplexer as a block controller is possible. To do this we have used a parity preserving reversible gates for circuit design. Since the ever increasing demand for communication will soon exceed today's performance limit, it is interesting to study ways of reducing cost and increasing speed along with increasing operations. Knowing that all the circuits have nano dimensions, it is clear that the nanotechnology will plays an important role in the future developments.

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