Parallel modular technologies in digital signal processing

Igor Anatolyevich Kalmykov, Konstantin Aleksandrovich Katkov, Naumenko Daniil Olegovich, Artem Bronislavovich Sarkisov, Alena Vasilyevna Makarova

North-Caucasian Federal University, Str., Kulakova, 2, Stavropol, 355029, Russia

Abstract: The research objective is to increase the rate of performing the digital signal processing (DSP) operations. It is possible to achieve this objective due to the computing parallelism. The work shows, that for ensuring real-time signal processing the algebraic structures which exhibit the ring and field properties, are to be used, particularly the residue number system (RNS) and the polynomial system of residue classes (PSRC). The application of the new modular technologies in the DSP tasks allows not only increasing the computing rate, but also ensuring the correct result achievement under the influence of disturbances during the data communication and an equipment failure due to the operation - level parallelism and low-bit data processing.
[Kalmykov I. A., Katkov K.A., Naumenko D., Sarkisov A.B., Makarova A.V. **Parallel modular technologies in digital signal processing.** *Life Sci J* 2014;11(11s):435-438] (ISSN:1097-8135). http://www.lifesciencesite.com. 98

Keywords: Digital signal processing, residue number system, polynomial system of residue classes, error correction, positional characteristics.

Introduction.

The present stage of applying the computing devices in signalling and signal processing systems has shown that the use of the digital signal processing (DSP) methods makes it relatively easy to provide high noise immunity of the data processing systems, the required accuracy and resolution, the simple conjugation of processing subsystems, the stability of the information processing chain parameters and some other advantages [1-3]. At the same time the digital signal processing tasks require real-time performing a great amount of the large-scale data computing.

The qualitative changes in the performance of the modern data transmission and processing systems could be achieved by applying the new DSP mathematical model, which supports parallel computing. At the same time, such DSP technology should not only improve the rate and accuracy of the signal processing, but also provide the fault-tolerance of a computing device of the digital signal processing [3-6].

Body. The importance of the DSP tasks makes it worthwhile to develop specialized processors (SP) for its solution. At the same time, the digital signal processing system performance is to the large extent determined by the DSP mathematical model.

Nowadays all the SP DSP feasibilities use several mathematical models which could be divided into the following groups. The basis of the first one is formed by the mathematical models based on implementing the orthogonal signal conversions over the complex number field, particularly the Discrete Fourier Transform (DFT) and the Fast Fourier Transform (FFT). Thus, in the broadband wireless access (BWA) systems the orthogonal frequency division multiplexing (OFDM) technology is applied for the disturbance control upon the multipath reception. The OFDM method is technically feasible by performing the Inverse Discrete Fourier Transform (Fast Fourier Transform, FFT) in a transmitter modulator and the Forward Discrete Fourier Transform - in the receiver demodulator of a transmitter-receiver [1-3].

The residue number system (RNS) is suggested to use in order to increase the rate of such orthogonal transformations performing. In this case, the A number is represented as a set of residues, $A=(a_1, a_2,...,a_n)$, where $A \equiv a_i \bmod p_i$;

i =1,2,…,n, obtained by dividing it into the pairwise relatively prime moduli p_i. The RNS main advantage is the high-speed performance of modular operations, which include addition, subtraction and multiplication [3-7]. In case two numbers A and B are represented in the position-independent modular code $A=(a_1, a_2,..., a_n)$ and $B=(b_1, b_2,...,b_n)$, then the operations of addition, subtraction, and multiplication could be reduced to the respective operations on residues

$$\begin{aligned} A+B &= ((a_1+b_1)\bmod p_1, (a_2+b_2)\bmod p_2,\ldots,(a_n+b_n)\bmod p_n), \\ A-B &= ((a_1-b_1)\bmod p_1, (a_2-b_2)\bmod p_2,\ldots,(a_n-b_n)\bmod p_n), \\ A\cdot B &= ((a_1\cdot b_1)\bmod p_1, (a_2\cdot b_2)\bmod p_2,\ldots,(a_n\cdot b_n)\bmod p_n). \end{aligned} \quad (1)$$

Then, using the residue number system the orthogonal signal conversions could be carried out in the form of n concurrently performed Discrete Fourier Transform computing.

$$\begin{cases} X(k)\bmod p_1 = \left|\sum_{l=0}^{N-1} \left||x(l)|_{p_n}^{+}\cdot|W^{lk}|_{p_1}^{+}\right|_{p_1}^{+}\right|_{p_n}^{+} \\ \vdots \\ X(k)\bmod p_n = \left|\sum_{l=0}^{N-1} \left||x(l)|_{p_n}^{+}\cdot|W^{lk}|_{p_n}^{+}\right|_{p_n}^{+}\right|_{p_n}^{+} \end{cases}. \quad (2)$$

where W^{lk} - is a twiddle factor;

k =0,1,2,…,N-1; $N = 2^v$.

The SP RNS circuit implementation, shown in the Figure 1, is required in order to perform the expression (5). The specific feature of such special-purpose processor is the presence of *n* computing chains which operate concurrently and independently. In each of them the orthogonal signal conversions are performed by the respective module.

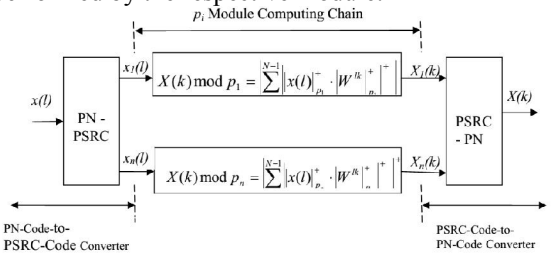

Figure 1 - Structure of the RNS Parallel Special-Purpose Processor

The operation - level parallelism allows attributing this special-purpose processor to the SIMD type. Using a single instruction flow, which is simultaneously sent to all computing chains, the computing device performs orthogonal conversions according to (2). A low-bit number of residues, the absence of data exchange between computing chains, allow increasing the special-purpose processor performance compared with the classical architecture of the signal processors. In this case it is enough to increase the number of computing chains, i.e. the RNS bases, in order to improve the computing accuracy.

The computing chain circuit implementation could be constructed in accordance with the selected DSP algorithm. Thus, using the FFT parallel-pipelined algorithm the expression (2) will be

$$X(k) \bmod p_i = \left| \left| \sum_{n=0}^{N/2-1} x_{v-1,0}(n) W_N^{2nk} \right|_{p_i}^{+} + \left| \sum_{n=0}^{N/2-1} x_{v-1,1}(n) W_N^{2(n+1)k} \right|_{p_i}^{+} \right|_{p_i}^{+}. \quad (3)$$

where $x_{v-1,0}(n) = x(2nT),\ x_{v-1,1}(n) = x((2n+1)T)$ - is a sequence of even and odd numbers, respectively; $W_N^2 = e^{-\frac{2\pi}{N/2}}$.

Along with the modular operations for carrying out parallel computing in the position-independent codes two non-modular operations should be performed. For any parallel SP DSP, operating in RNS, one of the mandatory non-modular operations is the forward conversion from the positional notation (PN) to the RNS code. Since the division operation is not defined in RNS, the residue computing is usually reduced to a set of modular operations. The conducted studies have shown that the algorithms, based on the direct summation method have less time expenditures [7,8].

For performing a conversion it is necessary to calculate the constant values, which are the equivalents to the degrees 2^j and factors at the corresponding base powers of a_j, represented in RNS $a_i = \sum_{j=0}^{v-1} (a_j 2^j) \bmod p_i$, where $v = \lceil \log_2 p_i \rceil$.

The second mandatory procedure is the conversion from the RNS code to the positional code. Nowadays while implementing the position-independent computing devices the retroversion method, based on the Chinese Residue Theorem (CRT), has been most widely spread [6-8].

In this case, the conversion task is represented as follows - for a given set of modules it is necessary p_i, $i = 1,2,...,n$ to perform the conversion of the *n*-dimensional image $A = (a_1, a_2, ..., a_n)$ in the based system $P = \prod_{i=1}^{n} p_i$ so, that the condition will be fulfilled.

$$A = a_1 B_1 + a_2 B_2 + ... + a_n B_n - r_A P, \quad (4)$$

where $B_i = m_i \prod_{\substack{j=1 \\ j \neq i}}^{n} p_j$ - are the orthogonal bases of the PSRC system; $m_i \prod_{\substack{j=1 \\ j \neq i}}^{n} p_j \equiv 1 \bmod p_i$ - is the weight of the orthogonal basis; r_A – is the number rank.

The comparative analysis of the FFT performing time in the positional system T_{pn}^{FFT} (T1), and using the parallel computing T_{RNC}^{FFT} (T2) is shown in the Figure 2. For assessing the relative factor has been chosen $K = \frac{T_{PN}^{FFT}}{T_{RNC}^{FFT}}$.

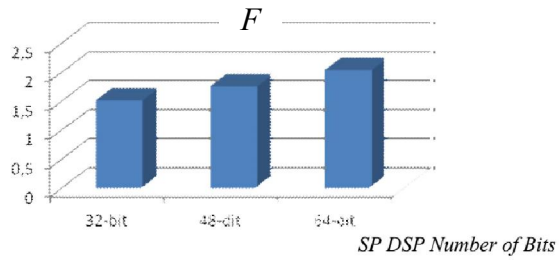

Figure 2 - Comparative Analysis of the FFT Performing Time in PN and RNS

The analysis of the Figure 2 shows that the use of the modular code allows increasing the digital signal processing rate using the FFT algorithm by more than 1.5 times. Moreover, upon increasing the bit number of the processed data the payoff raises. Thus, while the 64-bit data processing the position-independent processor speed is more than twice as much as the speed of the SP DSP

positional one, even subject to the necessary of performing the operations of the forward and inverse code conversion. Further improving the SP DSP performance could be possible through the implementation of the orthogonal signal conversions in the polynomial ring [9-11]. Let us have a polynomial ring *P(z)*, with the factors in the form of the field elements *GF(p),* which determines the accuracy of the orthogonal signal conversions computing. In case the ring is decomposed into a sum of the local rings P_l(z) of polynomials, formed by the irreducible polynomials $p_l(z)$, i.e. $P(z) = P_1(z) + P_2(z) + ... + P_n(z)$, *; l=1, ..., n*, than in this system there is an orthogonal conversion, which is generalized DFT, if the following conditions are fulfilled:

1. $b_l(z)$ - the primitive element of the *d* order for the local ring P_l(z).

2. *d* has the multiplicative inverse d^* element, i. e. $d^* d = p^v - 1$.

Then the orthogonal signal conversion will be

$$\left(X_1(l),...,X_n(l)\right) = \left(\sum_{j=0}^{d-1} x_1(j) b_1^{jl},...,\sum_{j=0}^{d-1} x_n(j) b_n^{jl}\right), \quad (5)$$

Equating the coordinates, we will obtain *n* pairs of the DSP forward conversion

$$\begin{cases} X_1(l) = \sum_{j=0}^{d-1} x_1(j) b_1^{jl} \bmod p_1(z) \\ \vdots \\ X_n(l) = \sum_{j=0}^{d-1} x_n(j) b_n^{jl} \bmod p_n(z) \end{cases}, \quad (6)$$

where

$$x_i(j) \equiv x(j) \bmod p_i(z);\ b_i^{\pm jl} \equiv b^{\pm jl} \bmod p_i(z), X_i(l) \equiv X(l) \bmod p_i(z)$$

Applying the expression (6) allows reducing the orthogonal signal conversions computing in the Galois field over the ring *P(z)* to *n* independent computing carried out by the modules p_i(z) of the polynomial code of the residue classes (PCRC). In this case the PCRC application allows not only increasing the data processing rate, but also ensuring the restore of the distorted results which arise from the SP DSP failures.

If the range of the possible change in the encoded set of polynomials is restricted, in other words, *k* is chosen from the *n* PCRC bases ($k < n$), it will allow dividing the entire Galois field range *P(z)* into two disjoint subsets. The first subset is called the working range and is given, $P_1(z) = \prod_{i=1}^{k} p_i(z)$, and the second subset is defined by the product $r = n - k$ of the control modules $P_2(z) = \prod_{i=k+1}^{k+r} p_i(z)$.

The polynomial $A(z)$ with factors in the field $GF(p)$ will be deemed to be disposed if and only if $\deg A(z) < \deg P_1(z)$. Otherwise, $A(z)$, submitted to PCRC is considered to be erroneous.

Thee absence of relationships between the computing chains of the PCRC processors do not allow the errors to move on the other grounds. In this case, the change in the error multiplicity does not lead to the error propagation both among the bits within the base and from one base to another.

In the work [9] the researches of the corrective abilities of the modular codes have been conducted. For correcting a single error it is necessary to introduce into the ordered PCRC for which $\deg p_1(z) \le ... \le \deg p_k(z)$ is true, two control bases $p_{k+1}(z)$, $p_{k+2}(z)$ satisfying

$$\deg p_{k-1}(z) + \deg p_k(z) \le \deg p_{k+1}(z) + \deg p_{k+2}(z), \quad (7)$$

Let the error has occurred by the module p_i(z). In this case, the error changes the residue value $a_i(z)$ by an amount of $\Delta a_i(z)$, so that $a_i^*(z) = a_i(z) + \Delta a_i(z)$ is obtained. In this case, the polynomial $A(z) = (a_1(z),...,a_i(z),...,a_{k+2}(z))$, belonging to the working range is converted into a forbidden polynomial $A^*(z) = (a_1(z),...,a_i^*(z),...,a_{k+2}(z))$, lying outside the operating range. For performing the error detection and correction operations the positional characteristics are used. Thus, in the works [9,10] the positional characteristic of the polynomial normalized trace is used. For correcting an error in the work [11] the algorithm for the bases system extension is suggested. In the work [12] the algorithm for computing the positional characteristic - the factors of the generalized polyadic notation is used. In this work we have considered the positional characteristic - the interval number, which is determined by dividing the polynomial *A(z)* by the working range P_l(z). But the division operation in PCRC has not been defined, so the interval calculation should be reduced to a set of the modular operations.

$$l(z) = \left\lfloor \frac{A(z)}{P_1(z)} \right\rfloor = \left\lfloor \frac{\sum_{i=1}^{k+2} a(z) B_i(z) + r_A P(z)}{P_1(z)} \right\rfloor = \left\lfloor \frac{\sum_{i=1}^{k+2} a(z)\left(R_i(z) + B_i^*(z)\right) + r_A P(z)}{P_1(z)} \right\rfloor =$$

$$= \left(\sum_{i=1}^{k+r} a_i(z) R_i(z) + \left\lfloor \frac{\sum_{j=1}^{k} a_j(z) B_j^*(z)}{P_1(z)} \right\rfloor + \frac{r_A(z) P(z)}{P_1(z)} \right) \bmod P(z), \quad (8)$$

where $B_i(z) = R_i(z) P_1(z) + B_i^*(z)$ - is the orthogonal basis of the complete PCRC bases system;

$B_i(z) \equiv B_i^*(z) \bmod P_1(z)$ - is the orthogonal basis of the irredundant PCRC bases system, built using the work bases; $r_A(z)$ – is the polynomial rank *A(z)*; $P(z) = \prod_{i=1}^{k+2} p_i(z) = P_1(z)P_2(z)$ - is the entire PCRC range.

Since the set of values of the interval number *l(z)* is the $P_2(z)$ moduli ring, than the expression (8) takes the form of

$$l\ (z) = \left(\sum_{i=1}^{k+r} a_i(z) R_i(z) + r_A^*(z) \right) \bmod P_2(z), \quad (9)$$

where the rank of the irredundant system is determined by the expression

$$r_A^*(z) = \left[\frac{\sum_{j=1}^{k} a_j(z) B_j^*(z)}{P_1(z)} \right]. \quad (10)$$

If the result of the expression (9) is zero, then the result obtained by modular SP DSP contains no error, otherwise - there is an error in the computing outcome. At the same time such redundant modular code could correct all the single errors and more than 90 percent of double errors.

Conclusions.

The work shows the appropriateness of using the parallel computing for the DSP implementation. The application of the position-independent modular codes subject to the independent parallel low-bit residue processing, allows reducing the time expenditures required for performing FFT compared with the positional special-purpose digital signal processor. In addition, the PCRC use also allows ensuring the detection and correction of the errors which could occur during the SP DSP operation.

Corresponding Author:
Dr. Kalmykov Igor Anatolyevich
North-Caucasian Federal University,
Str., Kulakova, 2, Stavropol, 355029, Russia

References

1. Rohde & Schwarz, 2008. R&S FSQ-K96 OFDM Vector Signal Analysis with the R&S FSQ Signal Analyzer. Product Brochure.
2. Yong S. C., J. Kim, W. Young and G. Chung, 2010. Kang MIMO-OFDM Wireless Communications with MATLAB, WILEY.
3. Shahana T., B. Jose, R. James, K. Jacob and S. Sasi, 2008. RRNS-convolutional encoded concatenated code for ofdm based wireless communication. In Networks. 16th IEEE International Conference, pp: 1–6.
4. Keller T., T. Liew, and L. Hanzo, 2000. Adaptive rate RRNS coded OFDM transmission for mobile communication channels. In Vehicular Technology Conference Proceedings, VTC 2000-Spring Tokyo.
5. Hosseinzadeh M., K. Navi and S. Gorgin, 2007. A New Moduli Set for Residue Number System. Electrical Engineering, ICEE'07. International Conference on. 11–12 April 2007, pp: 1–6.
6. Goh V. T. and M. Siddiqi, 2008. Multiple error detection and correction based on redundant residue number systems, Communications, IEEE Transactions on, 56(3): 325 –330.
7. Chervyakov, N.I., I.A. Kalmykov, V.A. Galkina, Y.O. Shchelkunova, and A.A Shilov, 2003. Elements of Computer Mathematics and Neuroinformatics. M.: Fizmatlit, pp: 216.
8. Katkov K.A. and I..A. Kalmykov, 2013. Application of Parallel Technologies in Navigation Management under the Conditions of Artificial Ionospheric Disturbances World Applied Sciences Journal 26 (1): 108-113.
9. Kalmykov, I.A., A.V. Zinoviev, and Y.V. Emarlukova, , 2009. High-Speed Systolic Fault-Tolerant Digital Signal Processors for Information and Communication Systems. Information and Communication Technologies, 7(2): 31 – 37.
10. Kalmykov, I.A., A.B. Sarkisov, E.M. Yakovleva, and M. I. Kalmykov, 2013. Modular Systolic Digital Signal Processor of Reconfigurable Structure. Bulletin of the North Caucasus Federal University, 2: 30-34.
11. Kalmykov, I.A. and A.B. Khayvatov, 2007. Mathematical Model of Fault-Tolerant Computing Facilities Operating in Polynomial System of Residue Classes. Information and Communication Technologies, 3: 39-42.
12. Kalmykov, I.A. and Lobodin, 2007. Development of Inverse Transform Algorithm for Position-Independent Adaptive Information Security Tools. Information and Communication Technologies, 3: 146-159.

7/9/2014