Impact of Clocking Sources on Electro-Magnetic Interference in Digital FPGA Chips

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Abstract: Electro-Magnetic Interference (EMI) has been a challenging issue on the designs of a high-speed printed circuit board (PCB) and digital circuits. The EMI emitted from a chip can produce incorrect signaling due to the EM noises that change the value of signal lines routed on the chip itself or the PCB. The EMI problem becomes much more critical when the circuit speed increases. In a modern high-performance digital chip, its clock frequency is normally more than a GHz. Moreover, supply and threshold voltages have been shrunken continuously. Consequently, a digital chip is more likely to produce malfunction due to the EMI noises coupled with correct values of signals. In this paper, we investigate the EMI of a traditional digital circuit, particularly on the circuits implemented on a commercial FPGA chip. We focus on the impact of a clock frequency of a chip and an off-chip oscillator on an emitted EMI.
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1. Introduction

In a modern high performance computing era, signal integrity and power integrity have become a critical problem that should be solved for the secure operations of digital chips [1,2]. The EMI sensitivity of signals increases as semiconductor technologies are advanced because of reduced supply and threshold voltages in modern CMOS technologies. Moreover, a clock frequency of high performance chip is usually more than 1 GHz and the number of transistors is around billion [1]. In this circumstance of chip operations, the quantity of EM noise has been increased and now the EMI problem should be solved for a correct and secure chip operation. The correct and secure operations are very demanding criteria in embedded real-time system used in a car safety system, aerospace safety critical applications, etc.

In particular, the EMI issues are getting much attention in modern vehicular and consumer electronics where radio-frequency (RF) communications can interfere with signaling and logic operations of circuits. The EM noises radiated from the chip operation can interfere with RF operations so that radio devices in the electronics components can work in a wrong way.

Since a modern system-on-chip (SoC) includes digital blocks and noise-sensitive analog circuit blocks together on a single chip, EMI noises generated from each part can make critical impacts to the functionalities of other parts. Generally, EMI increases as a clock frequency and transistor integration density increase. At the same time, the immunity of chip operations decreases as nano-scaled technology advances [1]. In consequence, the EMI problem will be getting more serious in the future.

In order to cope with the EM noise problem, there have been many various researches in different level of designs: EM noise aware chip layout and board level EM reduction technique, etc. Off-chip and on-chip couple capacitance insertions have been considered as most simple and effective technique for EM noise reduction. The coupling capacitance provides stable power supply lines and reduces voltage noises on the power supply lines. In general, the ground bounce by voltage drop noises which is normally caused by high current consumption can be reduced by the coupling capacitance and it leads to EM noise reduction. However, the on-chip and off-chip coupling capacitance increase chip and PCB design cost. In particular, on-chip capacitance increases chip area and consumes more power (leakage power due to the wide area of the on-chip capacitance) [1]. In addition to the use of coupling capacitance, there have been many independent design approaches: low package inductance, EM-aware placement and routing, spread-spectrum clocking, and substrate isolation [1].

When an EM noise is concerned, a global clock is considered as a source of generating the noises due to the high and periodic current consumption at the clock edges which all the circuit elements are synchronized with for the stepwise synchronized working. In this paper, we are focusing a global clock related EM-noise because that the global related EM noise problem expects to be much more serious due to the higher clock frequency.

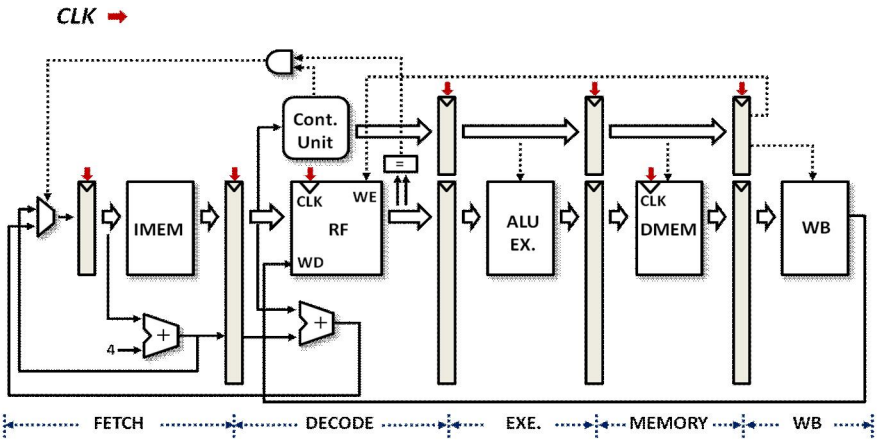

Figure 1. Experimental setting for detecting EM noise

In this paper, in order to provide a fundamental understanding of EM emission from a synchronous clock-based digital circuit, we investigate the EM emission while changing its working clock frequency. Through the investigation, we derived a fundamental property of the EM emission of a chip with respect to the clock frequency of the chip.

We use two difference clock generators for a chip: (1) *on-board oscillator*, (2) *digital clock manager* (DCM) in a Xilinx FPGA chip. The on-board oscillator is generally used in conventional PCB with or without programmability. The oscillator becomes main source oscillator reference clock for a system. The frequency of oscillator can be changed by on-chip internal PLLs or DLLs. In this paper, we have used different oscillators for different clock frequencies without PLL and DLL to see the pure EM effect of the frequency of on-board oscillator.

On the other hand, for the second experimental case, we use a Xilinx DCM IP module for transforming an incoming on-board oscillator clock signal to the target clock frequencies. With a fixed on-board oscillator, we can produce different clock frequency by manipulating the DCM module on an FPGA chip. Through the investigation of these two different cases, we can check the impact of clocking source of a digital chip on EM noises, particularly in a commercial FPGA chips.

Finally, we found that the EM emission from a chip is more depending on the on-board clock oscillator frequency than the actual working frequency derived from the on-board oscillator frequency.

2. EMI Experimental Hardware Setup

As a target digital circuit, we have designed a simple MIPS processor [3]. The Figure 1 shows the simple MIPS core architecture with 5 pipeline stages.

For evaluating EMI emitted from the FPGA chip implementing the simple MIPS core, we build an experimental setup with the following measurement devices.

- Oscillator Analyzer: Tektronix TDS5032B
- Spectrum Analyzer: Agilent E4402B
- Xilinx Spartan-3 XC3S400 FPGA Dev. Board
- FPGA Programmer & Notebook
- EM Probe: Beehive EM Probe Set

Figure 2 shows our experimental setup with the measurement tools. Probing EM emission from a chip that is located in the central part of the PCB is shown in Figure 3. The position of an EM probe has been searched to find out the position where maximum EM emission is observed.

For a test chip, we have designed a synchronous MIPS on a Xilinx spartan-3 FPGA chip with an on-board oscillator socket so that oscillators can be replaced easily. An EMI noise has been observed while varying clock frequency of the MIPS core from 20 MHz to 60 MHz by configuring "Digital Clock Manager (DCM) [4]" in Xilinx FPGA chip. On the other hand, in order to evaluate the impact of on-board oscillator, we have observed EMI emitted from a chip while varying the frequency of the on-board oscillator.

3. Results

At first, we have measured EM noises emitted from a chip when the chip is powered on but is doing nothing in order to find out the ground level EM noise. Note that an on-board oscillator has been disconnected from the FPGA chip. The noise level of EM emission from the dummy chip has been observed as 38 dBuV.

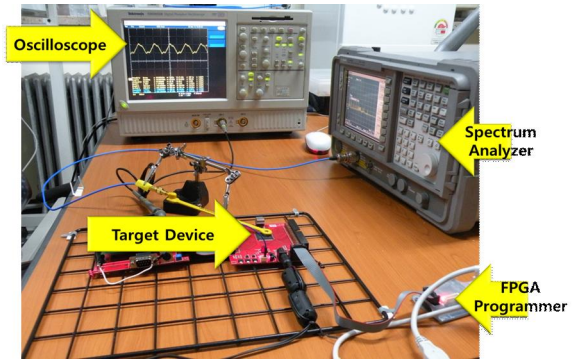

Figure 2. Experimental setting for detecting EM noise

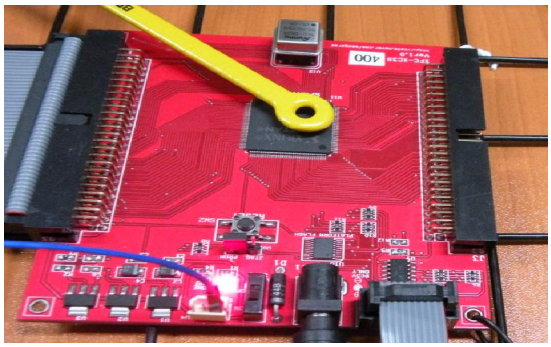

Figure 3. Probing EMI emitted from a chip

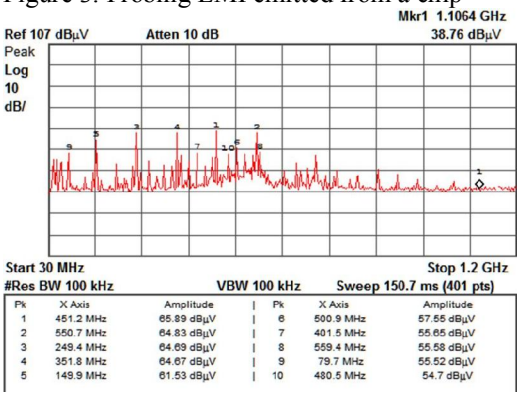

Figure 4. EM spectrum analysis for MIPS FPGA chip with 50MHz on-board oscillator and 20MHz DCM on-chip clocking.

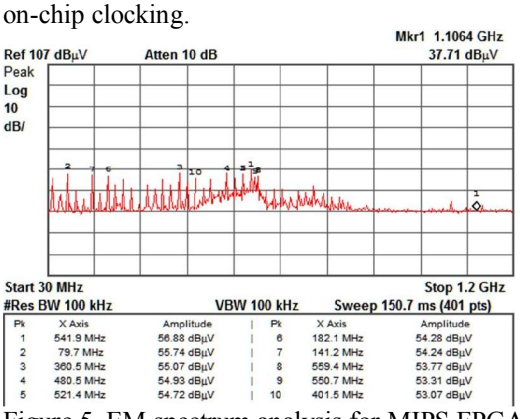

Figure 5. EM spectrum analysis for MIPS FPGA chip with 20MHz on-board oscillator / on-chip clocking.

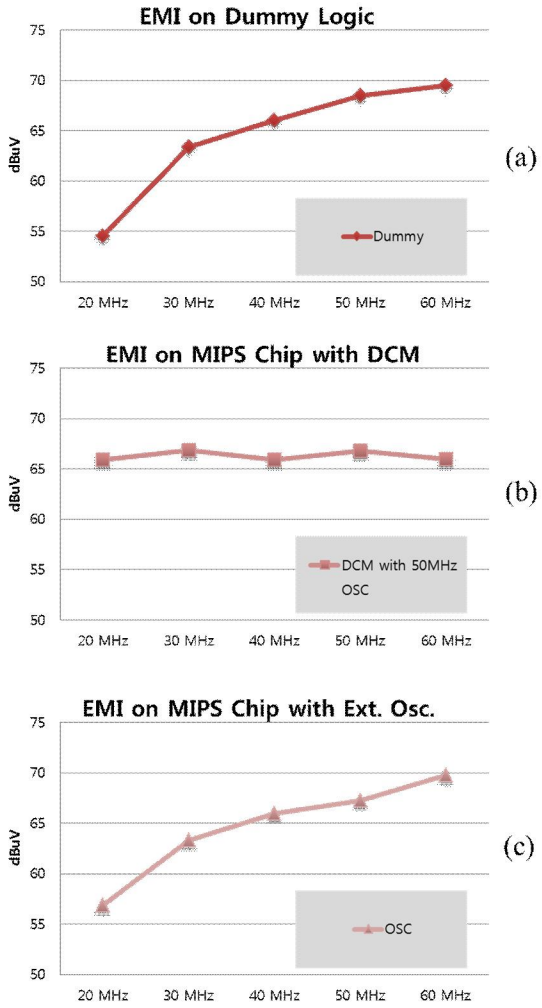

Figure 6. EMI from the three different working chips: (a) EMI radiation from dummy logic clocked with on-board oscillators whose frequencies are 20MHz, 30MHz, 40MHz, 50MHz, and 60MHz, respectively. (b) EMI radiation from MIPS FPGA chip with an on-board 50MHz oscillator but working frequency of the MIPS chips vary from 20MHz to 60MHz, (c) EMI radiation from the MIPS FPGA chip with on-board oscillators whose frequencies are 20MHz, 30MHz, 40MHz, 50MHz, and 60MHz, respectively.

Then, we have connected an on-board oscillator to a chip and we have made the chip working at the frequency range from 20 MHz to 60 MHz. As shown in Figure 6(a), EMI increases from 54.51 dBuV to 69.5 dBuV as we increase the frequency of the on-board oscillator from 20 MHz to 60 MHz, respectively. Through this experiment, we can build a first-order fitting equation as follows.

$$EM\ Strengh = 0.6086 \times Osc\text{-}Freq + 0.1082$$

The actual voltage of EM noises increase faster than linearly since the EM noise is generally evaluated in a log scale. As a second experimental case, we use single clock frequency (50MHz) from an on-board oscillator but we generate different clock frequencies (20 MHz to 60 MHz) from the oscillator frequency (50 MHz) by reconfiguring a Xilinx DCM. Figure 4 shows EM spectrum analysis for MIPS FPGA chip with 50MHz on-board oscillator and 20MHz DCM on-chip clocking. As shown in Figure 4, radiated EMI is much more strongly related with the frequency, 50MHz, of on-board oscillator rather than the clock frequency, 20 MHz, produced by a DCM. The Xilinx DCM transforms a given oscillator frequency to the frequency what we want to use by reconfiguration. In this case, as shown in Figure 6(b), the strength of EM noise is not changed much and almost constant EM noise level is observed even when the clock frequency generated from a DCM varies.

Then, as a third experiment, we change the frequency of an on-board oscillator itself. One of experiments with a 20MHz on-board oscillator clock is shown in Figure 5. Unlike the second case but like as the first case, the quantity of EM noises increase as the frequency changes. The EM strength is almost similar to the observation in our first experiment as shown in Figure 6(c).

4. Discussions

The key observation of our experimental study is that the strength of the EM emission from a chip is strongly depending on the on-board oscillator. In general, the actual working clock frequency seems to be key factor affecting the level of EM noise. However, through our experimental investigation, we observed that the frequency of an on-board oscillator actually has a stronger impact on EMI than that of the actual working clock frequency of a chip.

To further verify our results more precisely, we need to build a chip with more gates/transistors since chip size can be another factor of emitting different EMI. This will be possible future work. Finally, EMI radiation impact of a clock generated from an on-chip ring oscillator will be another interesting future work.

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