Implementation of Reconfigurable Fault Tolerant Network on Chip for Aerospace Applications

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Abstract: The reliability of the software chip is the essential factor in VLSI design since the chip can be implanted in any embedded circuit varies from simple adder to crucial satellite device. Thus breach in VLSI chip operation may results in huge negative impact devastation. A novel architecture of VLSI chip testing design is proposed and unlike from normal BIST structure this structure ensures the safety of entire aircraft by monitoring the flow of signals around aircraft and controlling various part of the system for better security. ERRIC architecture is initially proven to be best testing and controlling structure for aircraft applications. Performance analysis of area, power, and timing constraints has been proved better using Quartus – II synthesizer tool. A method of Nios Processor controlled aircraft safety is ensured as a new proposal. Nios processor design has the unique advantage of high accuracy and flexibility over reconfigurable Network on chip applications.
[A. Karthikeyan, P. Senthil Kumar, V. Parthasarathy. **Implementation of Reconfigurable Fault Tolerant Network on Chip for Aerospace Applications**. *Life Sci J* 2013;10(2):2823-2835] (ISSN:1097-8135). http://www.lifesciencesite.com. 391

Key words: BIST, ERRIC, NIOS, Aero space, NoC

1. INTRODUCTION

A Novel architecture of protecting value resource of an aircraft including human lives has been proposed as aircraft testing and monitoring system. Due to various consideration like are, unconventional battery operated power and enormous loss which cannot be retried through a small delay defect will be occurred. A adaptive reconfigurable Nios II architecture is employed to achieve all the above constraints over existing ERRIC architecture, performance analysis of area, power, and timing constraints has been proved better using Quartus-II synthesis tool. Major device failure for frequent accident occurrences has been taken as area of interest, like wheel, altitude indicator, and gear shifter for wing flops. All the tested circuitry methods are proved to be proved to be effective using a pseudo random exhaustive test pattern generator. Fault Tolerant Control (FTC) for aircraft systems has received considerable attention from the control engineers in the past couple of decades. The inspiration behind this attention is to build safer and more reliable aircraft systems that can sustain the effect of failures. The need for fault tolerant control methods is therefore critical.

A fault is defined as “malfunction” of any physical component or a sub-system that results in its failure to perform as designed. The main reasons for faults in aircraft systems are:

- Natural wear and tear of mechanical or electrical components.
- Eternal unknown catastrophic disturbances, and
- Improper maintenance of electro-mechanical components.

It is highly desired that when a fault occurs, it is timely detected and is informed to both pilot and autopilot to take necessary action. This timely response to faults reduces any disastrous consequences. For this reason, fault detection and isolation methods received considerable attention from both control and signal processing communities in the last couple of decades (13,19) for an extensive survey on various methods for fault detection.

Fault Tolerant NoC (FT-NoC) system specifically designed for the control of aircraft parts by implementing redundancy in the topology of the NoC thus increasing reliability. In doing so, we review the architecture of the elements inside a NoC system; classify various faults and redundancy types to implement fault tolerance; and briefly mention various parts of an aircraft attempting to map the structure of an aircraft within the design of a FT-NoC system for aircraft control.

Networks-on-Chip (NoCs) have been proposed as a promising solution to complex on chip communication problems. Every chip design has four major aspects:

- Computation
- Memory
- Communication and
- Input/output.

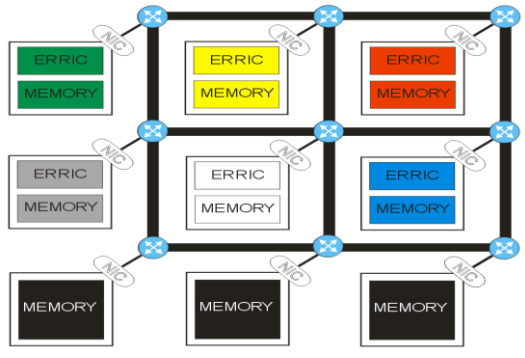
The main focus of this work is to design and implement a synthesizable NoC, which can evaluate the tradeoffs between different architectural and

algorithmic designs like: router architecture, switching techniques, topology architecture and routing algorithms. The main components of the proposed NoC Framework includes: Processing Element (PE), Instruction (I-MEM) and Data Memory (D-MEM), Core and Network Interfaces, Router, and the Channel. Ever increasing requirements on electronic systems are one of the key factors for evolution of the integrated circuit technology. Continuous technology scaling has made it possible to integrate billions of transistors on a single chip.

In order to cope with the growing needs of the interconnected infrastructure the Network on Chip (NoC) concept has been introduced which benefits computer systems by providing higher levels of performance and reliability. Such computers are now a mandatory component in the design of automatic control units for aviation systems.

1.1 PROBLEM DEFINITION

One of the most important advantages in designing NoC for multiprocessor systems is that the information which is inserted in the system from any input element (sensors, etc) or headed to an output element (altimeter, etc) are directly connected to their respective processing units. The main disadvantage of the 2D-Mesh system is the delay on the system incurred by the routing paths. And even though the cockpit, the most important unit with centric functions, is placed in the centre of the matrix topology, some hop-count delays from the centered unit are still present. The each major aircraft structural element presented in Figure 2.1(a) has its own color coded functional unit. Parts with similar traffic pattern and functions are placed as close as possible to each other to reduce the network overhead and decrease the hop count during packet transmission. For state condition recording purposes and to keep the formation



resemblance, two extra memory blocks are used.

Figure 1.1(a) FT-NoC fixed Mesh Topology

Based on the objectives, each major aircraft element is mapped onto a functional unit in the NoC. Each unit consists of the processing unit (Embedded Reliable Reduced Instruction Processor - ERRIC), the local memory and any other necessary IP block.

1.1.1 ERRIC PROCESSOR

A ERRIC architecture is used to detect ad tolerate the Error occurrences in a Embedded circuit. A mesh topology data sharing system is utilized by the ERRIC structure as a NoC core. To counter the reliability challenges inside the processing units of a NoC system we use the Embedded Reliable Reduced Instruction Computer (ERRIC). The instruction set for this processor is specially designed malfunction tolerant and fail-safe for permanent faults. This maximizes performance and reliability of the NoC since the reliability of a system is based on the reliability of its components. Ability to tolerate malfunctions invisible for the rest of the system is crucial as the ratio of malfunction/permanent faults in aerospace. The ERRIC basic elements for instruction manipulation are shown in Figure 1.1(b) .

They include a Control Unit (CU) to decode an instruction and fetch the next one, Register Files (RF) to keep data, and separate Arithmetic Unit (AU) and Logic Unit (LU) to execute arithmetic and logic functions. The extra hardware blocks check inputs and recover from any detected fault (marked with a bright colour in Figure). Structural redundancy used to achieve malfunction tolerance is about 13%. The error recovery is only activated when a fault has been detected so the power consumption stays as minimum.

The ERRIC is divided to passive and active zones enabling the application of different redundancy techniques. The operands are checked during operation and if not damaged the operation is performed with the result either stored back into the RF with extra information inserted for future checking, or, if output, it is transmitted to memories or external I/O devices. The ERRIC is a 32 bit architecture, and is able to fetch 2 instructions in every fetch cycle which reduces the execution time to nearly half that of other processors.

1.1.2 Drawbacks

- Due to the embedded nature of the ERRIC architecture, the flow of signal cannot be Reconfigured dynamically. If a ERRIC structure is designed for a particular aircraft design, it cannot be dynamically modified for different aircraft
- The main draw backs of mesh topology system are the delay on the system incurred by the routing paths.
- There are high chances of redundancy in many of the network connections.
- Overall cost of this network is way too high as compared to other network topology.

- Set-up and maintenance of this topology is very difficult. Even administration of the network is tough

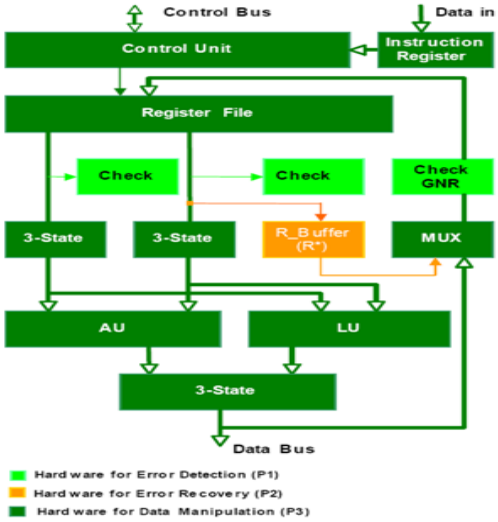


Figure 1.1(b) ERRIC structure

1.2 PROPOSED APPROACH

A VLSI structure based Nios II processor architecture is employed to replace the ERRIC structure. Due to the FPGA implementation rather than Embedded structure it has the unique advantage of dynamic reconfiguration of signal flow, this will be high speed. Ring topology is included for NoC structure the expected speed and accuracy will be comparatively high. This paper focuses on monitoring the various parts embedded to the Aircraft engine and Aircraft flight.

Having a centric unit when architecting a system entails the implementation of a star network topology with the central unit, in this case the cockpit switch, being directly connected to all units thus decreasing the hop count in routing paths and increasing the bandwidth available over each directly connected link.

However, the star topology's main disadvantage is its low fault tolerance due to a link failure or a switch crash resulting in whole network crashes and all communication between the various components stopping. Under these conditions the system software will have the ability to reconfigure the topology when a fault in the links is detected. The system can modify the architecture and switch it to ring in four cases:

- If a fault is detected over any of the star links the redundant ring links will come out of stand by and form a shortest path to the central switch. · If a link is jammed due to traffic congestion and shortage of bandwidth in a link the central switch will attempt to form another path to the destination and start load balancing over the directly connected and the redundant links.
- To decrease the switching load in the central processor when the source and destination of transmissions are adjacent, the central switch will bring up the direct link amongst them thus avoiding the communication through it (useful for writing information into the Black Box).
- If the central switch malfunctions the topology will change completely to ring formation and the idlest processing unit will take the control of the network. The system states will then return to the latest healthy status of the network stored in the Black Box memory. The system architecture for a FT-NoC is shown in Figure 1.2. In this case e ach functional unit relates to a part of the aircraft and is integrated with a direct connection from its switch to the processing units, the ERRIC, and another direct connection to the memory elements inside that unit. These connections guarantee that for as long as a memory or a processor is still available in the system, the whole system can continue to function. The major technical aspects and design consideration of this system are:
- The functional units are composed of a processing unit (ERRIC processor structure), a local memory module and their corresponding Intellectual Property (IP) blocks. IP blocks import and export data from and to the peripheral instruments or ADC/ DAC sensors.

Structural redundancy is realized in the black box memory architecture through two sets of redundant links connecting it to the central switch. The six links form a star topology as the main active formation in the system. Redundant links are placed in the system to enable embedded architecture reconfigurability and load balancing in the network by forming a ring topology inside the NoC system chip.

- The system software implements a generalized algorithm of fault tolerance, known as GAFT, to detect permanent links or switches and reconfigure the network if necessary.
- The functional units with similar tasks and traffic patterns must be placed as close to each other as possible to enable direct communication between them.
- Even though the use of straight links reduces the delay on the network by keeping the lengths of these links short implementing such straight links must be avoided so as to reduce crosstalk on the links connecting the central unit to each functional unit.
- Real time system Recovery Point (RP) could be stored as a part of the Black Box. Such specific computer system design and architecture for aircraft control systems will provide.

- Low levels of power consumption in the system
- Parallelism in hardware and wire speed by increasing the available resources
- Reliable system for sensitive computation through implementation of fault tolerance in various levels
- Low levels of system maintenance by providing auto-reconfigurability Compatibility with previous system architectures and designs installed in current Fly-By-Wire (FBW) systems.
-

1.2.1 NIOS II Processor Advantage

- In the ERRIC processor standard (fixed) architecture we can't reconfigure the structure.
- In the Nios processor is an dynamic reconfigure architecture we can adopt any kind processor.
- With the help of Nios processor we can reduce the logic elements.
- Execution speed is fast then ERRIC processor

Table 1.1 Comparison of core in NIOS II processor

Feature		Core		
		Nios II/e	Nios II/s	Nios II/f
Objective		Minimal core size	Small core size	Fast execution speed
Performance	DMIPS/MHz	0.15	0.74	1.16
	Max, DMIPS	31	127	218
	Max, fmax	200MHz	165 MHz	185 MHz
Pipeline		1 stage	5 stages	6 stages
External address space		2 GB	2 GB	2 GB without MMU 4 GB with MMU

2 Literature Survey on Robust Fault – Tolerant Control for Aircraft System

The need to design controllers that guarantee both stability and performance upon the occurrence of faults has been an active area of research. To address this problem, in this thesis we present different methodologies to design robust controllers that guarantee both stability and robustness for actuator faults and uncertainties. In the first part of this paper, we introduce the classical uncertainty formulation using Linear Fractional Transformation (LFT) and describe LFT's special cases-norm bounded and convex polytopic uncertainty descriptions. Practical methods to formulate these uncertainty structures are described. In the same spirit, formulation of faults and their modeling for robust control system design is provided. In the second part of this thesis, we demonstrate the application of a Luenberger observer for fast Fault Diagnosis and Isolation (FDI). We describe the methodology to design a robust optimal control for actuator faults and present controller reconfiguration mechanism based on switching for the design of Fault Tolerant Control (FTC). System with both norm bounded uncertainties and actuator faults is formulated and an analytic method to and a robust stabilizing and guaranteed cost reliable controllers are also mentioned. To the end, we implement designed linear controllers in Boeing 747 (B747) non- linear system. We also denoted and evaluate potential problems that arise in switching based FTC and their effect on the closed loop nonlinear system. Robustness of linear controllers in nonlinear B747 was evaluated using excessive Monte Carlo simulation and results are presented.

3 VLSI IN AEROSYSTEM

The accidents have been happened due to various failure factors in aircraft varies from pilot mistake to circuit fault. The result of an accident affects the society with emotional and economic brutality. As small contributions to safety purpose an extensive digital protection circuit is designed using Nios II VLSI architecture.

Digital circuits are evolved to an cenpercented growth such that humans are entirely dependent on it for daily basis. Many parts of the aircraft like wheel, gear and altitude controller has been monitored using digital controller chip. The functionality of the aircraft parts can be detected but a intelligent analysis of what the necessary count measure must be taken care. A novel Nios II architecture VLSI chip is substituted to replace the ERRIC architecture for high fault coverage.

A digital VLSI chip ha to meet the following consideration when operating in adaptive, un conventional situations. Main constraints are

- Area
- Power
- Operating speed

Due to the battery operated power constraint, the power dissipation of the VLSI must be very low, as well like are and speed response. The delay time must be reduced to achieve high efficient chip design.

3.1 AIRCRAFT ACCIDENTS IN AVIATION

Weather-related aviation accidents, in both large and small aircraft, still remain one of the most significant causes for concern in aviation safety today, despite all the research and development which has been carried out over the last hundred years since the Wright Brothers first flew at Kitty Hawk Field. Accident and casualty statistics show a steady downwards trend in the number of accidents per year from approximately 1972. The accident records show that 2007 was a particularly safe year. In fact, 2007 was the second safest year since 1942 for airline accidents. In 2007, a total of 26 fatal multi-engine airliner accidents occurred. This resulted in 750 fatalities and 41 ground fatalities. The average for the ten year period from 1997-2007 was 34 fatal accidents, resulting in 914 fatalities. This steady decreasing trend in the number of airline accidents is despite the increase in passenger miles and in the context that growth in the aviation industry is expected to be approximately 3-5% per year.

3.1.1 Weather related accidents

High wind and driving rain was reported at the time the MD-82 attempted to land and subsequently skidded off the runway. It ran though a low retaining wall then broke into two parts and caught fire engulfing some passengers. The visibility was reported to be very poor at the time the pilot attempted to land the aircraft. Whilst the cause of the accident has not been officially determined, it is believed that wind shear may have been a strong contributing factor. Wind shear has been a factor in many aircraft accidents over the years for both large and small aircraft.

3.1.2 Wind shear and turbulence

Turbulence is similar to wind shear in that it can disturb the aircraft's attitude about its major axes but it does not tend to displace the aircraft from its intended flight path. They can be both transient and sporadic. Graphic evidence of a change to the intended path of an aircraft, which has encountered strong wind shear and turbulence during the landing and take-off sequences, has been captured on film on a number of occasions.

Thunderstorms can also produce very violent downdrafts known as micro bursts. These downbursts are very dangerous and have been the cause of many aircraft accidents and incidents over the years, and generally occur with thunderstorms originating in warmer climate areas. It is the very rapid change in wind speed and/or direction, which poses a real threat to an aircraft on its landing approach or on take-off. Close proximity to the ground leaves very little safety margin for recovery and a safe touchdown.

3.1.3 Educational methodology

This is essential to a safe and uneventful flight. It is customary to begin each meteorology lecture at UniSA by examining and analyzing the current weather information, and to look for conditions which were similar to those present, when an accident or incident occurred somewhere around the world. Repeated exercises such as this serve to reinforce, especially to inexperienced student pilots, the value of constant awareness and understanding of meteorological events. Graphic videos, CDs and DVDs are also used to help the student relate the practical aspect with the theory. This helps considerably with the early recognition of weather situations, which may change and develop to the point where it is too late to take avoiding action, often with disastrous consequences.

4 AIRCRAFT ARCHITECTURE

In the conventional aircraft architcture, the main part of the fuel is converted in propuslive power (primary power) by the engine; the remaining part (secondary power) is converted in mechanical hydralic, pneumatic and electrical form. The secondary power is destributed around he engine and airframe to supply all theon board systems as fo examples (ref below fig.) landing gear, braking and flight control system, air conditioning, pressurization, de-icing and avionics, etc., Therefore on the majority of the today's in-service aircraft of any size, either civil or military, secondary power is distributed by complex power distribution nets aboard, with an appropriate redundancy of all the systems for safety purpose. In order to reduce this complexity, with the aim to improve efficiency and reliability, the aircraft manufacturer's trend is towards the More Electric Aircraft (MEA) concept that is the wider adoption of electrical systems in preference to the others.

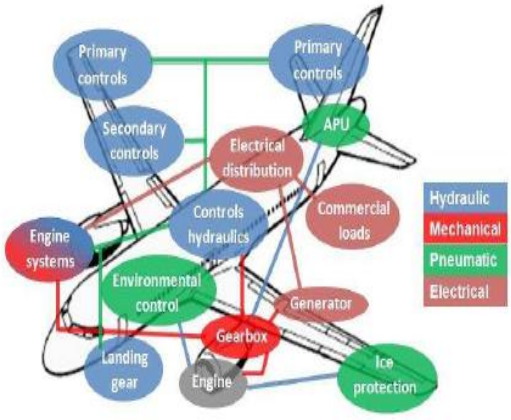


Figure 4.1 Schematic conventional aircraft

4.1 MAIN AIRCRAFT ON-BOARD SYSTEMS

The modern aircrafts are an integration of complex interacting technological components and powered by sophisticated power distribution architecture. Moreover, in order to guarantee high flight safety conditions, an appropriate redundancy of all the power connections is required. The conventional on-board secondary power distribution system of the modern civil aircrafts is schematically depicted in Fig.4.2 The main part of the fuel is converted into the aircraft propulsive power by the gas turbine engine. The remaining non-propulsive fuel is converted into four different secondary powers.

- Mechanical: transferred by the gearbox from the main gas turbine engine to the main electrical generator, to the central and local hydraulic pumps and to the other mechanically driven subsystems;

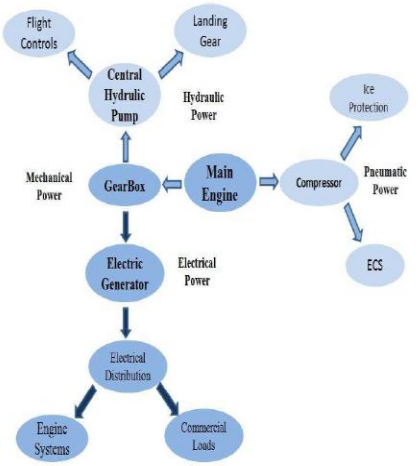


Figure 4.2 Schematic conventional aircraft power distribution system.

- hydraulic: transferred from the central hydraulic pump to the flight control actuators and to the ancillary systems;
- pneumatic: obtained by bleeding high pressure engines' compressors;
- Electric: obtained by the main electrical generator to supply all the electrical and avionics equipments.

4.2 FLIGHT SURFACE CONTROL

In the wings and in the tail of a wide-body aircraft there are several surfaces that the pilots can move/adjust in order to stabilize the airplane trajectory and to control the lift on the wings. Examples of these surfaces are reported in Fig.4.3. The adjustable surfaces can be sub divide in two groups with respect to their main functionality: the primary and secondary flight controls. The primary flight controls (ailerons, elevator and rudder) are used to control the roll, pitch and yaw even if they can perform secondary effects. In particular, the pitch control is exercised by four elevators located on the tail plane. Roll control is performed by two aileron sections located on the trailing edge of each wing. The yaw control is provided by three independent rudder sections located on the trailing edge of the vertical stabilizer. This control are associated with the aircraft yaw dampers, which is used to damp uncomfortable oscillation which can occur during flight. Each of these systems are powered independently by a dedicated actuator powered by the

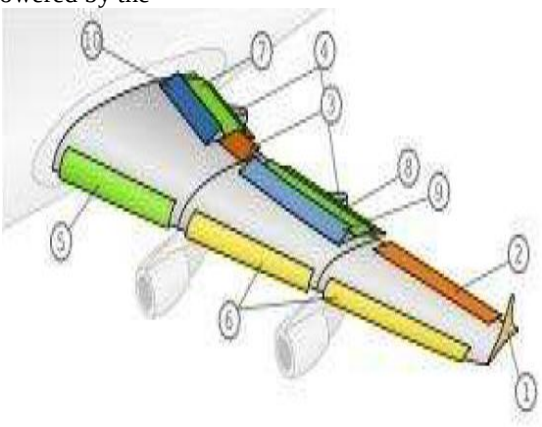


Figure 4.3 Wing control surfaces of a _fixed-wing aircraft:
1. wing-tip, 2. low speed aileron, 3. high speed aileron, 4. flap track fairing, 5. Kruger flaps, 6. slats, 7. three slotted inner flaps, 8. Three slotted outer flaps, 9. spoilers, 10.spoilers air-brakes.

Hydraulic systems. The secondary controls, also called high lift system, are used to Change the wing lift. It is performed by the flap control, which are positioned on the trailing part of the wing and are used to increase the wing area and camber. They are particularly used during the take-off or landing in order to change the lift for a given speed. The overall lift of the aircraft can also be performed by the slats which have the same function of the flap. In order to reduce the lift as well as increase the drag, the air-brakes are used and permit to the pilot to adjust rapidly his airspeed.

The number and type of actuators is very different, with respect to the considered aircraft. In addition, the load requirements are very different too, starting from few kilowatts for the edge slats, up to 50 − 60kW for the horizontal stabilizer and the rudders. Also the dynamic load profile can be quite different, there are few surfaces movements with very large extension and short duration (typically during the landing and take-off) or several `small' surface adjustments during the flight. In addition,

anomalous performances are generally requested to the actuators in critical flight conditions. Just for example, if all the engines on the same wing fail, the rudder has to be able to keep the rudder in a fixed position, with high yaw angle, during the flight. In this situation, very high torque is requested at the electric motor.

Figure 4.4 Primary control systems.

5 HARDWARE SPECIFICATIONS WITH FPGA

5.1 INTRODUCTION

- ModelSim is a verification and simulation tool for VHDL, Verilog, System Verilog, and mixed language designs. This lesson provides a brief conceptual overview of the ModelSim simulation environment. It is divided into four topics, which you will learn more about in subsequent lessons.
  1. Basic simulation flow
  2. Project flow
  3. Multiple library flow
  4. Debugging tools

1. Basic Simulation Flow

The following diagram shows the basic steps for simulating a design in Model Sim shown in fig.

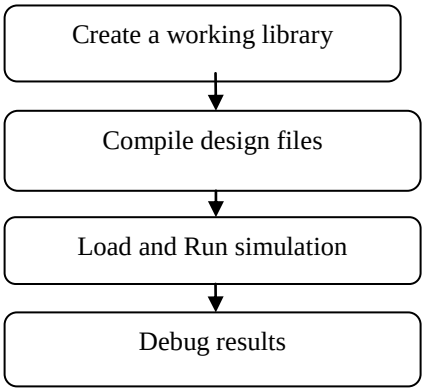


Figure 5.1 Basic simulation flow

A) Create a Working Library

- In ModelSim, all designs are compiled into a library. You typically start a new simulation in ModelSim by creating a working library called "work". "Work" is the library name used by the compiler as the default destination for compiled design units.

B) Compiling Your Design

- After creating the working library, you compile your design units into it. The ModelSim library format is compatible across all supported platforms. You can simulate your design on any platform without having to recompile your design.

C) Loading the Simulator with Your Design and Running the Simulation

- With the design compiled, you load the simulator with your design by invoking the Simulator on a top-level module (Verilog) or a configuration or entity/architecture pair (VHDL).
- Assuming the design loads successfully, the simulation time is set to zero, and you enter a run command to begin simulation.

D) Debugging your Results

- If you don't get the results you expect, you can use ModelSim's robust debugging environment to track down the cause of the problem.

5.1.1 Project Flow

- A project is a collection mechanism for an HDL design under specification or test. Even though you don't have to use projects in ModelSim, they may ease interaction with the tool and are useful for organizing files and specifying simulation settings.
- The following diagram shows the basic steps for simulating a design within a ModelSim project shown in fig.

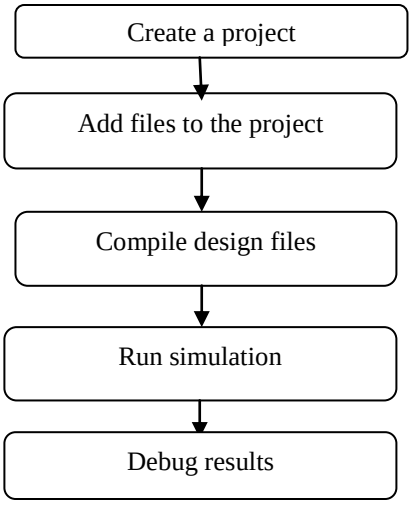


Figure 5.2 project flow

As you can see, the flow is similar to the basic simulation flow. However, there are two important differences. You do not have to create a working library in the project flow; it is done for you automatically. Projects are persistent. In other words, they will open every time you invoke ModelSim unless you specifically close them.

5.1.2 Multiple Library Flow

ModelSim uses libraries in two ways:

1) As a local working library that contains the compiled version of your design.

2) As a resource library.

- The contents of your working library will change as you update your design and recompile shown in fig. A resource library is typically static and serves as a parts source for design. You can create your own resource libraries, or they may be supplied by another design team or a third party.
- Specify which resource libraries will be used when the design is compiled, and there are rules to specify in which order they are searched. A common example of using both a working library and a resource library is one where your gate-level design and test bench are compiled into the working library, and the design references gate-level models in a separate resource library.

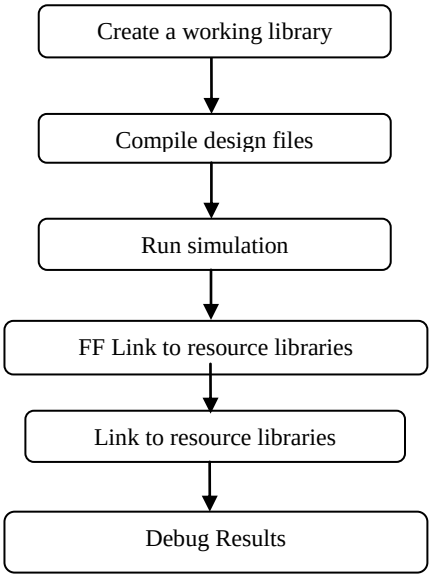


Figure 5.3 Multiple Library Flow

5.1.3 Debugging Tools

ModelSim offers numerous tools for debugging and analyzing your design. Several of these tools are covered in subsequent lessons, including

1. Using projects.
2. Working with multiple libraries.
3. Setting breakpoints and stepping through the source code.
4. Viewing waveforms and measuring time.

6 SIMULATION RESULTS

6.1 LINEAR FEEDBACK SHIFT REGISTER

In computing a liner feedback shift register (LFSR) is a shift register whose input but is a linear function of its previous state. The most commonly used linear function of single bits is XOR. Thus, an LFSR is most often a shift register whose input bit is driven by the exclusive-or (XOR) of some bits of the overall shit register value. The initial value of the LFSR is called the seed and because the operation of the register is deterministic, the stream of values produced by the register is completely determined by its current (or previous) state. Likewise because the register has a finite number of possible states, it must eventually enter a repeating cycle. However, an LFSR with a well – chosen feedback function can produce sequence of bits which appears random and which has a very long cycle. Applications of LFSR include generating.

- Pseudo – random numbers
- Pseudo – noise sequences
- Fast digital counters,
- Whitening sequences

Both hardware and software implementations of LFSR are common.

6.1.1 LFSR as a test pattern generator

Algorithmically generated test patterns for logic networks, while generally giving good fault coverage, have three disadvantages.

- Test pattern generation can be extremely time – consuming, particularly for sequential circuits.
- A good deal of storage is required by the tester to hold the test patterns.
- The speed at which tests can be applied is limited.

The limitation on testing speed mentioned above is caused by the necessity of storing test patterns in some secondary storage and retrieving them as tests are applied. Testing speed is important and not only because testing is a necessary step in a manufacturing line, but because it is often desirable to apply tests at operational speed. The problem of testing at operational speeds can be partially overcome by putting a high speed memory in the tester so that test patterns can be applied for short, high speed bursts. Nevertheless, these bursts are

relatively short nice blocks of patterns must still be retrieved from a secondary store.

An alternative to algorithmically generated tests which overcomes these disadvantage is the use of pseudo – random or pseudo exhaustive tests generated by an LFSR

A n-bit LFSR is a n-bit length shift register with feedback to its input. The feedback is formed by XORing or XNORing the outputs of selected stages of the shift register - referred to as 'taps' - and then inputting this to the least significant bit (stage 0). Each stage has a common clock. The 'linear' part of the term 'LFSR' derives from the fact that XOR and XNOR are linear functions. An example of a 5-bit LFSR is shown below:

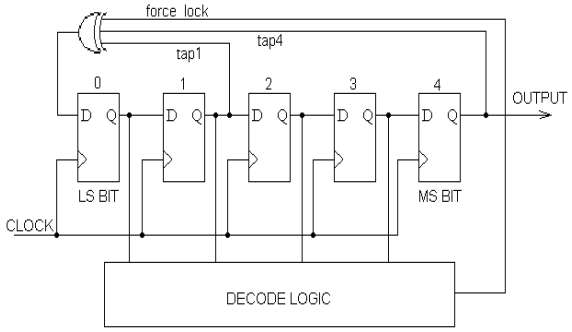


Figure 6.1 LFSR using 5 BIT

This has taps at stages 1 and 4 with XOR feedback. Note also that the LS bit of the shift register is, by convention, shown at the left hand side of the shift register, with the output being taken from the MS bit at the right hand side.

So what is it about a LFSR that makes it interesting? It will produce a pseudorandom sequence of length 2^{n-1} states (where n is the number of stages) if the LFSR is of maximal length. The sequence will then repeat from the initial state for as long as the LFSR is clocked.

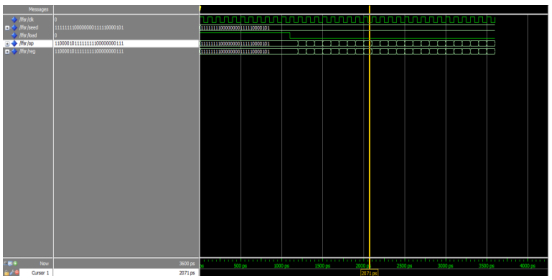


Figure 6.2 Simulation output for LFSR

Linear feedback shift register is a simple random pattern generation through a XORed feed. The above simulation results shows for 5 bit operation 1st and 4th bit will XOR and stored in MSB of 0th bit. The LFSR start to generate new test patterns for each positive edge of the clock pulse. LFSR is used to test the various aircraft parts.

6.2 SIGNATURE ANALYSIS

BIST techniques usually combine a built I binary pattern generator with circuitry for compressing the corresponding response data produced by a CUT. The compression techniques are Transition count, Syndrome checking, Signature analysis. The signature blocks compared the two sequences circuit under rest (cut) and look up table (LUT) that comparison output show in blow;

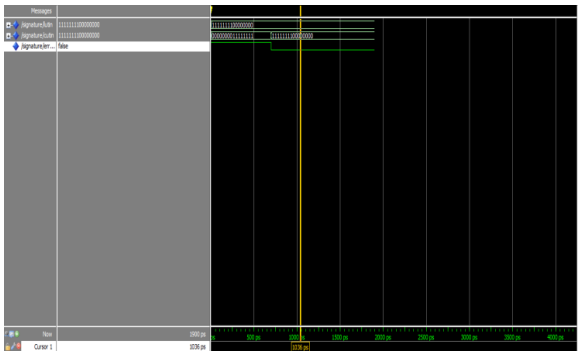


Figure 6.3 Simulation output for signature block

Signature analysis will be as an comparator in between the expected value and exact value of the wheel speed. The expected value will be in LUT look up table and exact value in CUT circuit under test. The LUT performance with the current actual device reading and is results both detected error and error ratio.

6.3 AIRCRAFT WHEEL ANALYSIS

In this section the environmental reference conditions (pressure, temperature, speed) of the front stages (fan, booster and compressor) of the GEnx, chosen has reference baseline engine for the trade-off study, are given. The take-off is considered the reference conditions for the thermo mechanical stresses of the entire structures (Sea Level Static max thrust, ISA2 Day +15◦C). This condition guarantees the maximum components operative temperatures in combination with the maximum shafts rotational speeds. The reference conditions for the embedded electrical machine design are:

- round per minutes at maximum speed:
  - ◊LP spool: 2581rpm
  - ◊ HP spool: 12946rpm
- round per minutes at idle speed:
  - ◊ LP spool: 565rpm
  - ◊ HP spool: 7957rpm

In Fig. 6.4 the typical torque, power and speed profiles for the HP shaft in the initial starting condition of the GEnx-1B are shown.

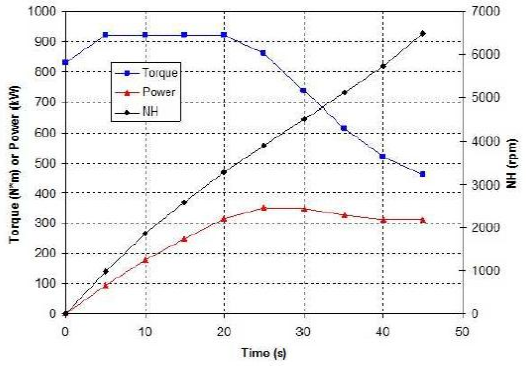


Figure 6.4 Torque, power and speed in the starting condition of the GEnx-1B.

Airplane tires are designed to withstand a wide range of operating conditions, including carrying very high loads and operating at very high speeds. It is common for a jet airplane tire to carry loads as heavy as 60,000 pounds while operating at ground speeds up to 235 miles per hour. To accommodate these operational conditions, each tire has specific load and speed rating. Tires are carefully designed and tested to withstand operation. Such way we make analysis to control the speed of the aircraft, if the speed is high or low than RPM, control and bring to normal value (RPM). Thus the output monitored and show in simulation result for low and high speed RPM of wheel

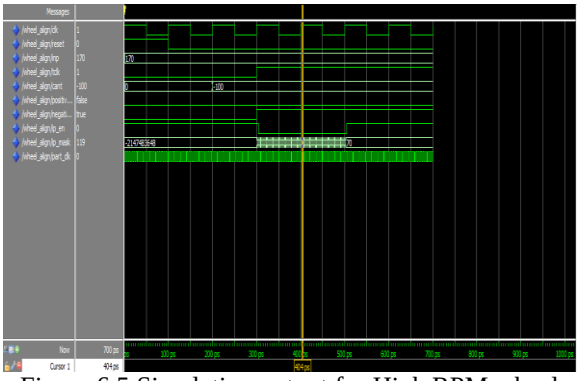


Figure 6.5 Simulation output for High RPM wheel

Wheel of the aircraft landing is settled of 70 rpm in case of any run time fault due to over voltage or any other defect, the expected rpm will be peaked in either positive or in negative direction, proposed controlling chip act as an voltage stabilizer by reading the motor rpm speed. Both the graphs shows the controlling voltage applied for high and low rpm of the wheel in aircraft.

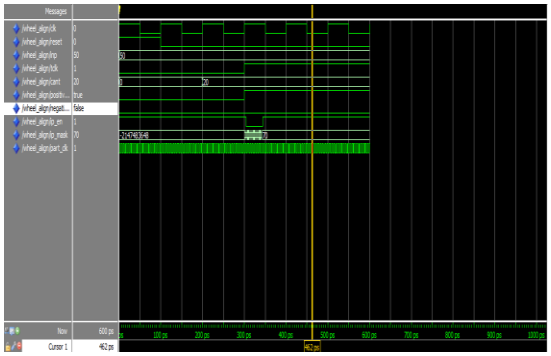


Figure 6.6 Simulation output for Low RPM wheel

6.4 ALTITUDE INDICATOR ANALYSIS

The ground proximity Modes are derived from a number of signal inputs to the computer; each input is received from a variety of aircraft system outputs including:

- Barometric air data
- Radio altitude
- Instrument landing system
- Attitude and heading reference system.

The source of these inputs to the computer will vary depending on aircraft type. Barometric air data includes altitude and vertical rate, or vertical speed. These two parameters are usually derived from an air data computer (ADC). This computer combines the functions of individual instruments, and can be used to determine data from the aircraft's pilot-static system:

- Altitude
- Vertical rate, or speed
- calibrated airspeed
- Mach number.

Air data computers usually have an input of total air temperature to enable computation of static air temperature and true airspeed.

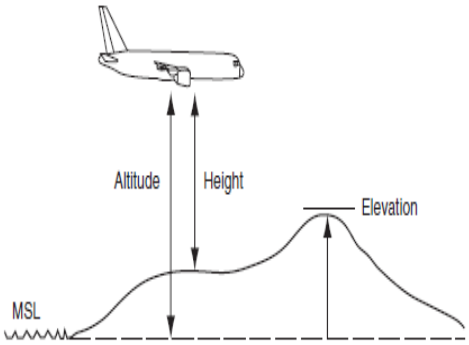


Figure 6.7 Elevation, altitude and height

It is important to differentiate between elevation, altitude and height. Referring to Fig. 6.7 the basic reference point is mean sea level (MSL). Terrain that rises above MSL is measured as elevation. The aircraft's altitude is measured (normally in feet) above MSL, whereas the aircraft's height is measured above the terrain. The attitude of an aircraft (pitch and roll) is sensed by gyroscopes. These sensors provide reference outputs that are processed to develop navigation and attitude data. Larger passenger aircraft derive this data from an inertial reference system (IRS). Developments in micro-electromechanical systems (MEMS) technology have led to silicon accelerometers that are more reliable and can be manufactured onto an integrated circuit. MEMS is the integration of mechanical elements, sensors and electronics on a common silicon substrate through micro-fabrication technology. This technology is being introduced onto general aviation aircraft for attitude and heading reference systems (AHRS).

An attitude indicator also known as ADI is used to inform the pilot of the orientation of the aircraft relative to earth. The glide slope indicator, indicating brown earth below and sky above, wings level horizon, in a slight nose-down attitude. If the aircraft dot is above the horizon line aircraft nose up if its below means nose is down. AI owered via in electrical motor, depends upon the speed of the motor attitude and motion will up or down level. In AI errors are caused by the movement of the pendulous vanes by centrifugal forces, resulting may affected the direction of movement in the aircraft. It will affected in the frequency level of navigations that monitoring in the cockpit.

6.4 GEAR SHIFT ANALYSIS

In the design of the embedded electrical machine, is mandatory to be competitive in terms of weight respect to the baseline solutions. The gearbox and generators weight of the conventional GEnx-1B solution are:

- Gearbox weight: 145kg;
- Generators\Starters weight: 2 × 103kg;
- In air craft's to move the flips is difficult. The flips movement depends upon the wind direction.
- According the wind direction the movement has to be set.
- To set the gear automatically we using the Gear shift.
- In this movement threshold shows the gear have to work for that wind direction and it will adjust the gear as required for wind direction.
- If the wind condition is high means gear level has to decrease and condition is low gear level have to increase.

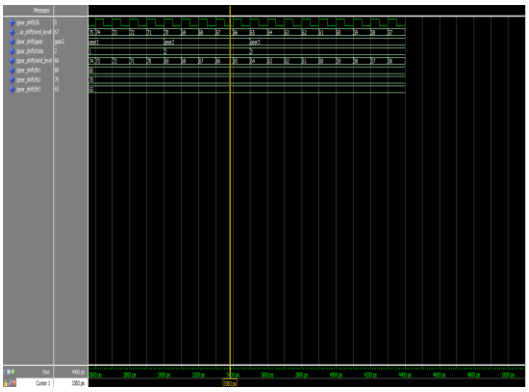


Figure 6.11 Simulation output for Gear Shift

The above simulation results shows the side fins of the aircraft is used to control the direction alignment of aircraft dedicated gearbox are employed to turn the fins into required angle and direction. The gear system s made to be automatic based on the air pressure in can of heavy pressure fins controlling will be under problem. Gear patterns need to be adjusted for smooth calibration of fins. That's shows in the above simulation results.

6.6. INTEGRATED OUTPUT

The below simulation results shows the integrated output for the all above three controlling his are connected through a star – ring hybrid topology and the performance graphs are shown.

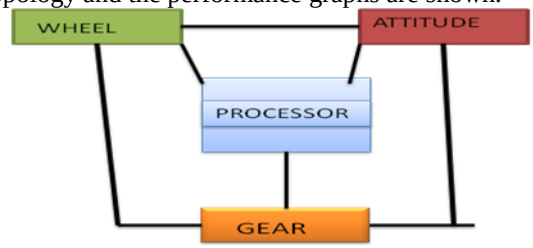


Figure 6.12 Mixed Topology

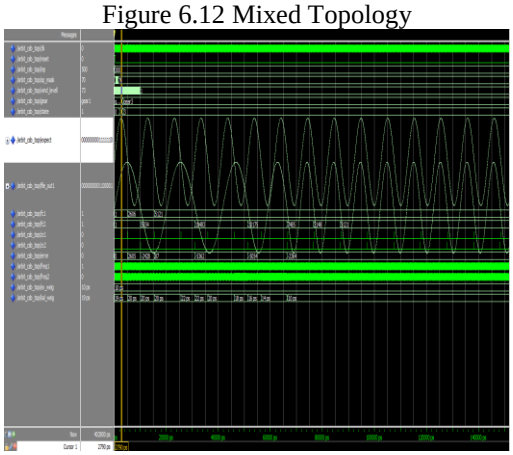
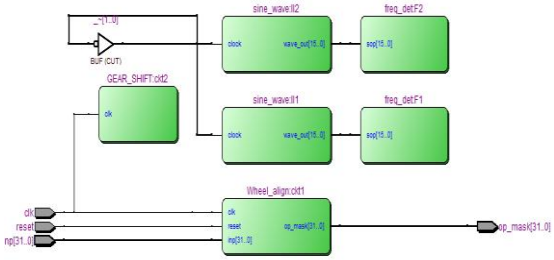


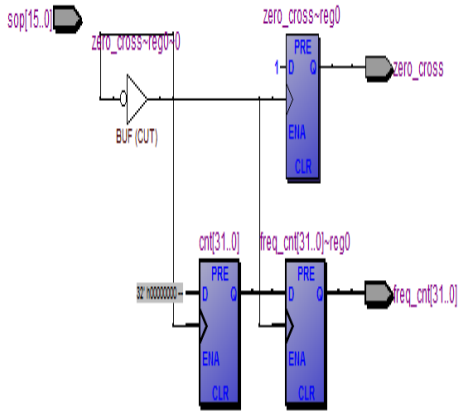
Figure 6.13 Simulation results for Integrated Output

7 RTL SCHEMATIC DIAGRAMS

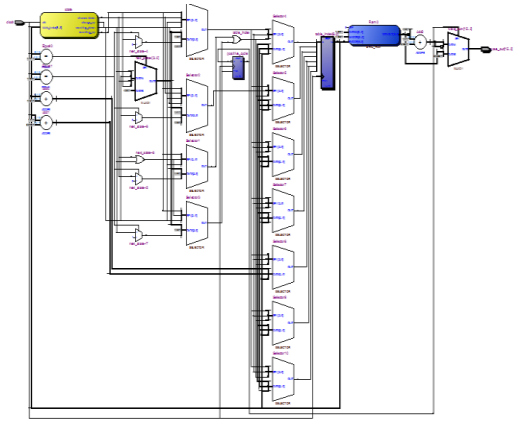
7.1 PROPOSE SYSTEM SCHEMATIC DIAGRAM



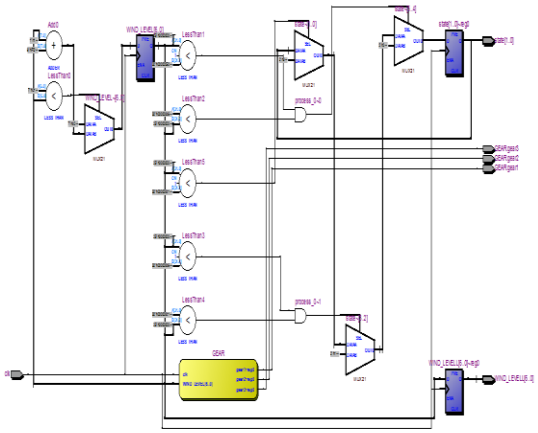
FR7.2 EQUENCY DETECTION



7.3 ALITUTDE SINE WAVE INDICATOR



7.4 GEAR SHIFT SCHEMATIC



8 PERFORMANCE COMPARISION

- In the ERRIC processor standard (fixed) architecture we cant reconfigure the structure.
- In the Nios processor is an dynamic reconfigure architecture we can adopt any kind processor.
- With the help of Nios processor we can reduce the logic elements.
- Execution speed is fast then ERRIC proces

8.1 LOGIC ELEMENT ANALYIZER

Logic element are the basic building blocks of FPGA device. Logic element has the unique capability to transform itself as and required gates. Logic elements consists of an LUT with Mux. The area of the chip is determined by the number of LE's ued in a HDL description. The below figure shows the LE's utilized in our proposed Nios II based aircraft test controller.

8.2 POWER ANALYIZER

Power dissipation of the chip will be calculated through the number of switching activity occurances in the cricital path of the digial circuit. Power and area of a chip are the major constriants which constributes to over all better performance.

8.3 TIMING ANALYIZER

Timing of a VLSI chip can be classified as three step

t_{su} - Set up time
t_{co} - Output time
t_{pd} - Propagation Delay

The chip performance will be calculated with the minimal and maximum delay prediction of Quartus II synthesizer. That shows in the below figure timing analysier.

9 CONCLUSION

A Hybrid architecture of integrating various controlling chips in through NoC is designed using VHDL description language. The Novel controlling design is modelled by analysing the cruical aircraft parts of wheels, fins, altitude meter. The performance evaluation of ERRIC and Nios II archtiecture is compared by means of logic elements utilized. The synthesixed result has been obtained using Quartous II synthesizer. Performance analyization of Area, Power, Time constrains has been proved better using Quartious II synthesis tool. The result concludes that propsed Nios II architecture yields 54% reduction in logic elements, which indirectry improves the speed optimizaion.

Architecture with fault	Logic Elements (Area)
ERRIC Processor	581
NIOS II Processor	321

Table 8.1 Comparision of Processors

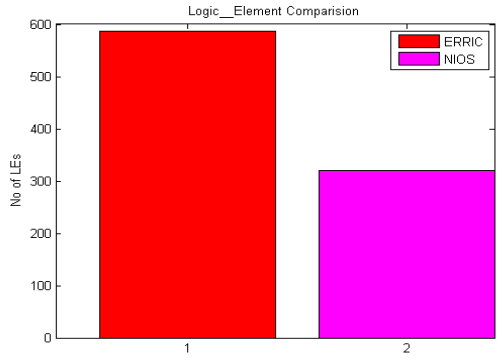


Figure 8.1 ERRIC vs NIOS II

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6/20/2013