Power Optimization In FPGA Routing Circuits

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Abstract: Power optimization is the paramount technique to reduce the power consumption in digital VLSI circuits. It is analyzed through relative analysis of the conventional FPGA routing technique with the proposed low-power FPGA routing technique. The proposed technique works in three various modes namely low-power, high-power and sleep mode. The FPGA switching circuitry shows reduced leakage power and area overhead in low power versus high speed mode. The conventional circuitry is reconfigured to surpass the existing method in terms of power and area. The simulation results show that the power dissipation in the proposed system is less than the existing system.
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1- Introduction

Field-programmable gate array is an Integrated circuit which is made up of Silicon. It is programmable at the customer's site after manufactured by the designer. Hence it is known as field-programmable gate array. It consists of programmable logic blocks which can be configured to perform both simple and complex logic functions and a programmable routing interconnect for implementing the above functions.It also consists of programmable I/O to interface the logic blocks and routing interconnect. FPGA's currently used in the semiconductor industry have logic components like memories, Arithmetic logic units and flip-flops arranged in rows or columns. The advantages of FPGA are performance, less expensive, reliable and easily marketable.

Power optimization is an efficient technique to reduce both static and dynamic power in the design of FPGAs in the future. In this paper, we propose a new routing switch which reduces the dynamic power consumption in contrast to the existing routing switch. The proposed Spartan-3 family FPGA can be used for various low-power applications. [3] [9]. The major power dissipated in an FPGA is due to the routing interconnect. In this paper, we propose two new routing switches which reduce both static and dynamic power dissipation.

The proposed Spartan-3 family FPGA can be used for various low-power applications. [3] [9]. The major power dissipated in an FPGA is due to the routing interconnect. In this paper, we propose two new routing switches which reduce both static and dynamic power dissipation. The two designs operate in three different modes namely high-speed, low-power and sleep mode. In low-power mode, both leakage and dynamic power are reduced by compromising speed. In high-speed mode, the power consumption is more than low-power mode. In sleep mode, leakage power reduction is more compared to low-power and high-power modes [1, 2].

2 - Background Theory

2.1- Routing Switch

Figure 1 illustrates the schematic diagram of a 6-T SRAM cell which consists of 2-PMOS transistors and 4-NMOS transistors. The four transistors which form two cross-coupled inverters are used to store each bit in SRAM. Two transistors known as access transistors are added to the 4-T cell for performing read and write operations (used to read data from SRAM and write data into SRAM). wl is the word line and bl is the bit line and blb is the output shown in Figure 1. V_{DD} is the supply voltage provided to the 6-T SRAM cell.

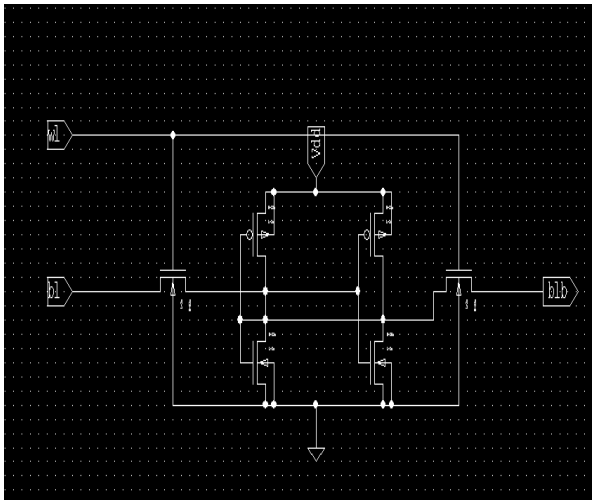

Figure 1. Schematic diagram of 6-T SRAM cell

SRAM cell is enabled by the word line which is used to control the access transistors. The bit

lines are used for reading and writing data from / into SRAM [8].

In high-speed mode, both PMOS and NMOS transistors are turned ON and the full-rail voltage V_{DD} is applied to the multiplexer which contributes to major dynamic power dissipation.

In low-power mode, the PMOS transistor is turned OFF and the NMOS transistor is turned ON. Since the output voltage is reduced by threshold voltage V_{TH}, the leakage power is minimized. In sleep mode, both the transistors are turned OFF. The total power dissipation in FPGA is due to static and dynamic power [8, 9]. Dynamic power dissipation is the major source of power dissipation in recent generation CMOS circuits [4].

Sub threshold leakage current and gate oxide leakage current are the foremost leakage techniques in recent generation Integrated circuits [7]. Sub threshold leakage current flows between source and drain of a MOSFET when the transistor is in OFF state ie., when the Gate voltage V_G is less than the threshold voltage V_{TH} of the transistor. Gate oxide leakage current flows due to tunneling current in a MOSFET. Tunneling current flows through the gate oxide layer of the transistor. As the oxide layer is made thinner,Gate oxide leakage current increases. Both types of leakage current increases as transistor width is increased. The programmable interconnection fabric component in FPGA occupies the major portion of transistor width, which is the major source of power dissipation [1, 8, 9].

2.2 - Low-power routing switch Design

The existing routing switch is illustrated in Figure 2. The routing switch consists of Static Random Access Memory (SRAM), multiplexer and Multiple threshold CMOS logic which is used for providing a supply voltage [5, 6]. The routing switch consists of NMOS and PMOS transistors connected in parallel [9].

In the proposed switch design, two sleep transistors are added in the pull-up network of the multiplexer to minimize the gate oxide leakage current [1, 9].

In low-power mode,multiplexer operates under a supply voltage of V_{DD} __ V_{TH} which reduces power dissipation. In high-power mode, supply voltage V_{DD} is given to the multiplexer. Hence the power dissipation is more in high-power mode compared to low-power mode. During sleep mode, both transistors are in OFF condition and hence it is known as sleep mode [9]. We use 0.18 micron CMOS technology in which the supply voltage V_{DD} varies from 1.8 to 2 V. We used 0.18 micron CMOS technology since it is the technology available with us in the place where research is carried out.

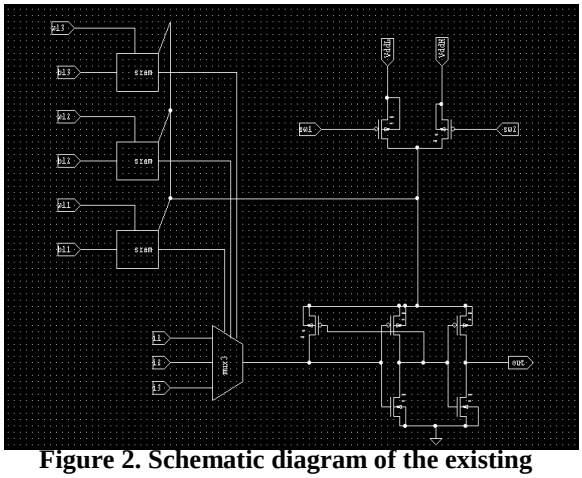

Figure 2. Schematic diagram of the existing routing switch

2.3 - Basic switch design

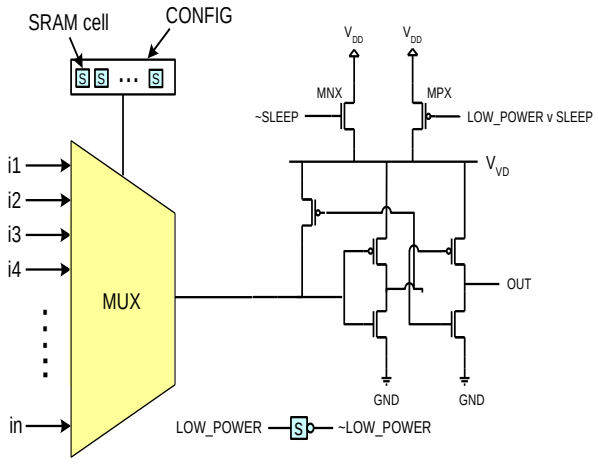

Figure 3. Basic switch design

Table 1. Different Modes of operation of the basic switch

Mode of operation	NMOS (MNX)	PMOS (MPX)
High speed	ON	ON
Low-power	ON	OFF
Sleep	OFF	OFF

Figure 3 and Table 1 illustrates the working of FPGA in all modes of operation namely high speed, low power and sleep mode, depending on the ON /OFF condition of NMOS and PMOS transistors [8].

Switching activity of transistor in high speed mode

In high-speed mode, both the transistors MNX and MPX are ON. Hence, a dual power supply is obtained across the routing switch as the circuit works in a symmetric triggering mode. Hence due to

symmetric triggering, the circuit works in high-speed mode.

Switching activity of transistor in low-power mode

In general, PMOS transistor contains majority carriers as holes and minority carriers as electrons where as in NMOS transistor majority carriers are electrons and minority carriers are holes. Since NMOS transistor MNX is turned on in this mode, mobility of electrons is more. For the movement of electrons, the power consumed is less than that is required for movement of electrons. Hence, it is known as low-power mode.

Switching activity of transistor in sleep mode

In sleep mode, both MNX and MPX transistors are turned OFF . The MUX output turns ON the routing transistors, but there is no power supply from MNX and MPX transistors. Hence the OFF condition of both transistors is known as sleep mode.

2.4 - High Speed Mode Operation

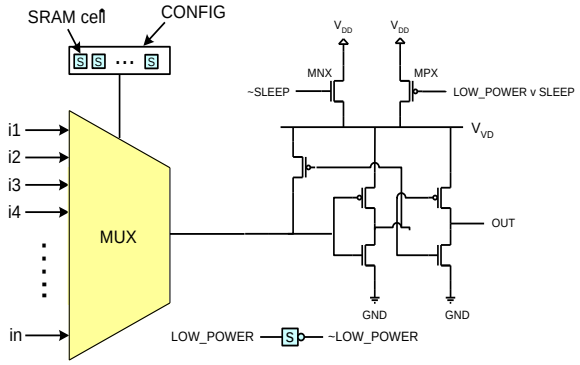

Figure 4. Basic switch design

Figure 4 shows the basic switch design and Table 2 illustrates the high speed mode of operation of the basic switch [8]. In the above figure**,** low-power mode indicates that the transistor MNX is turned ON and MPX is turned OFF. In sleep mode, both MNX and MPX transistors are turned OFF.

Table 2. High-power mode of operation of the basic switch

Mode of operation	NMOS (MNX)	PMOS (MPX)
High speed	ON	ON
Low-power	ON	OFF
Sleep	OFF	OFF

The circuit works on 1.2 V during low-power mode. The circuit works in 1.8V during high speed mode.In sleep mode, since there is no power consumption the circuit works in 0V. The typical values of power consumed by the circuit in three different modes are illustrated in [8].

2.5 - Low Power Mode Operation

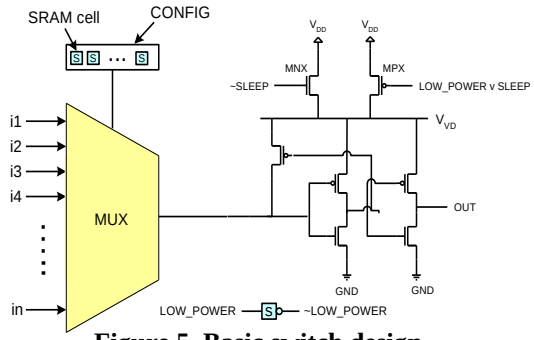

Figure 5. Basic switch design

Table 3. Low-power mode of operation of the basic switch

Mode of operation	NMOS (MNX)	PMOS (MPX)
High speed	ON	ON
Low-power	ON	OFF
Sleep	OFF	OFF

Figure 5 shows the basic switch design and Table 3 illustrates the low-power mode of operation of the basic switch [8]. In low-power mode of operation,the NMOS transistor MPX is turned ON and the PMOS transistor MPX is turned OFF,whereas both the NMOS and PMOS transistors are turned ON during high-speed mode of operation.

2.6 - Sleep Mode Operation

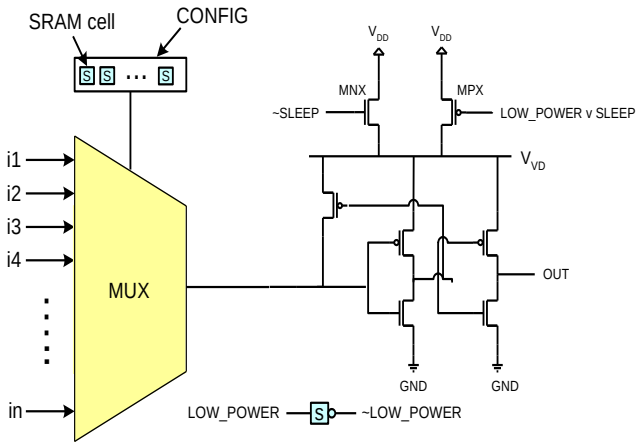

Figure 6. Basic switch design

Table 4. Sleep mode of operation of the basic switch

Mode of operation	NMOS (MNX)	PMOS (MPX)
High speed	ON	ON
Low-power	ON	OFF
Sleep	OFF	OFF

Figure 6 shows the basic switch design and Table 4 illustrates the sleep mode of operation of the basic switch [8]. In sleep mode both the NMOS and PMOS transistors are in OFF state. ie., The transistors goes into the sleep state.

3. Results

The simulation results are obtained using Xilinx software**.** Figure 7 and Figure 8 shows the power results of SRAM in Spartan 3e family and Spartan 6 family. The power results are obtained by analyzing the proposed routing switch in high speed versus low-power mode.

Table 5. Comparison of Spartan-3 and Spartan6 family

FPGA family	# of LUTs	# of FFs
Spartan-3	2	2
Spartan-6	4	8

Since current commercial FPGAs use either 4 LUT's or 6 LUT's (Look-up tables) we compared Spartan 3e and Spartan 6 families. The above table illustrates the number of LUT's and the number of FF's (Flip-flops) required for Spartan 3 and Spartan 6 families.

3.1 Power result of SRAM in Spartan 3e, Spartan 6 (base design)

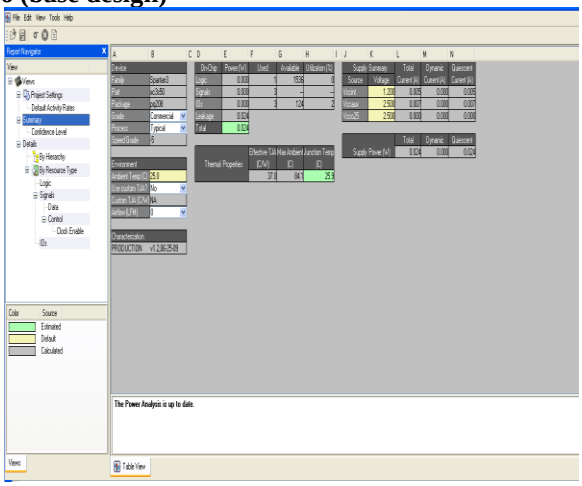

Figure 7. Power result of SRAM in SPARTAN 3e

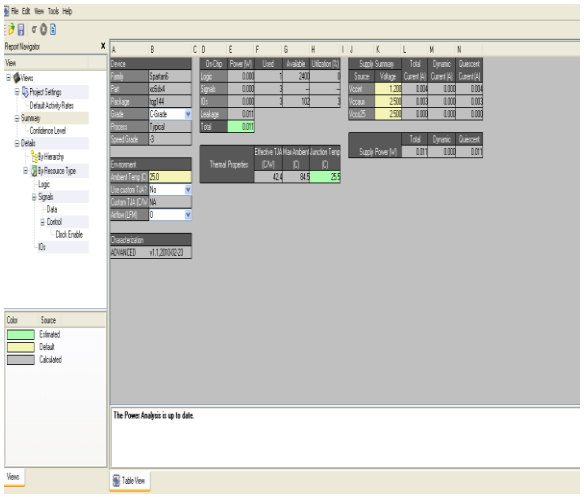

Figure 8. Power result of SRAM in SPARTAN6

From the analysis, the power consumption of the existing dual V_{DD} is 0.024W which has to be verified via SPARTAN 3e family and the same has to be analyzed for SPARTAN 6 which gives the power output 0.011W. In this analysis report the switching activity of the capacitor is not to the extent to change the behavior of the dynamic current. Power estimation has to be analyzed based on the transistor activity and it is observed based on vector-less analysis.The power results are synthesized using Xilinx (Verilog) and the simulation result of SRAM is obtained using Modelsim.

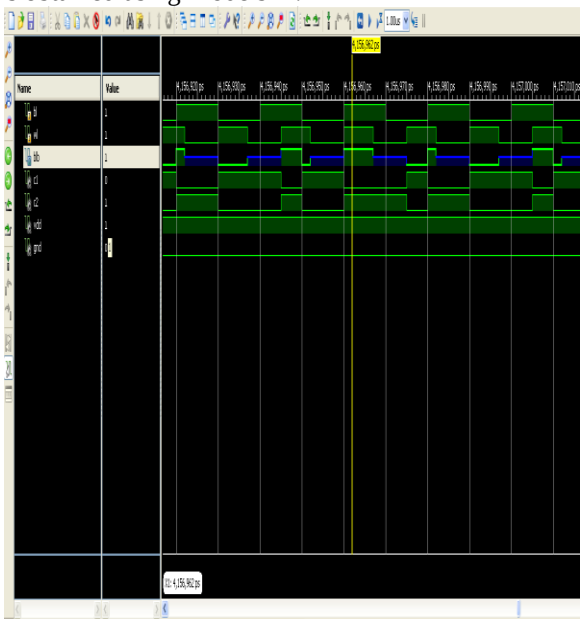

Figure 9. Simulation result of SRAM

As per the transistor design of SRAM, wl and bl are the inputs which terms to be word line and bit line of the SRAM design which produce the output at blb based on the bit value.

3.2 Power result of FPGA in Spartan 3e, Spartan 6 (base design)

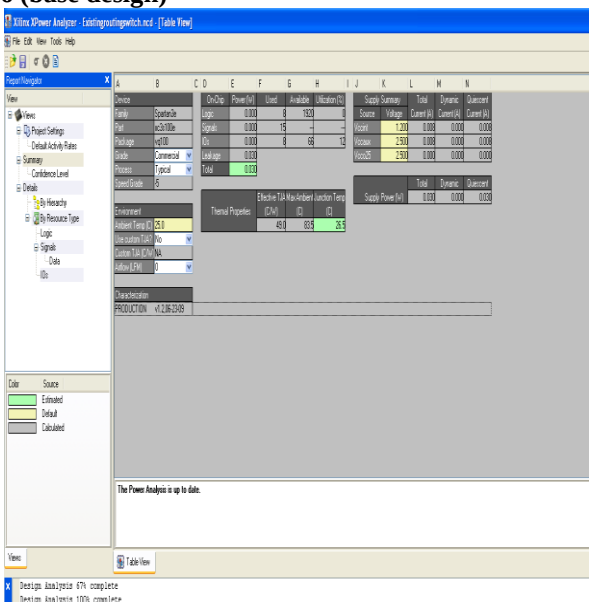

Figure 10. Power result of FPGA in SPARTAN 3e

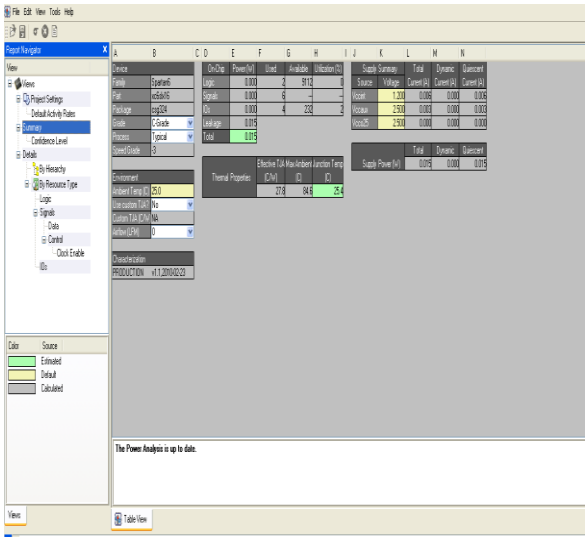

Figure 11. Power result of FPGA in SPARTAN 6

From the analysis, the power consumption of the existing dual V_{DD} is 0.030W which has to be verified via SPARTAN 3e family and the same has to be analyzed for SPARTAN 6 which gives the power output 0.015W. In this analysis report, the switching activity of the capacitor is not to the extent to change the behavior of the dynamic current. Power estimation has to be analyzed based on the transistor activity and it is observed based on vector-less analysis.

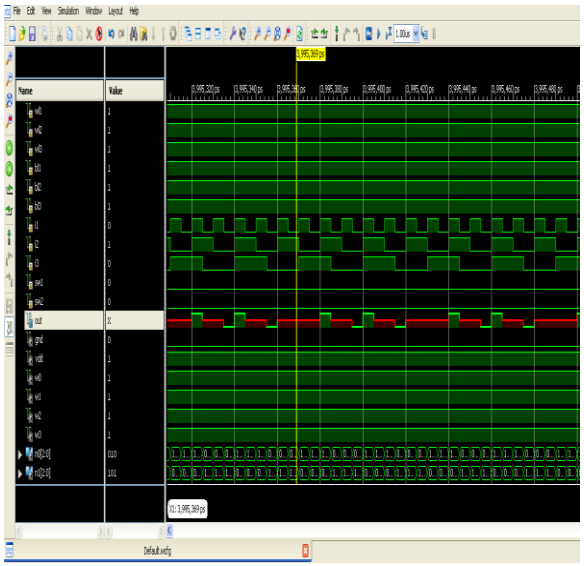

Figure 12. Simulation result of FPGA

As per the FPGA design, wl and bl are the inputs which terms to be word line and bit line of the FPGA design and sw1,sw2 are the switches which corresponds to Vdd-low and Vdd-high which produce the output at w based on the multiplexer configuration (select line).

3.2 Power result of SRAM in Spartan 3e, Spartan 6 (modified design)

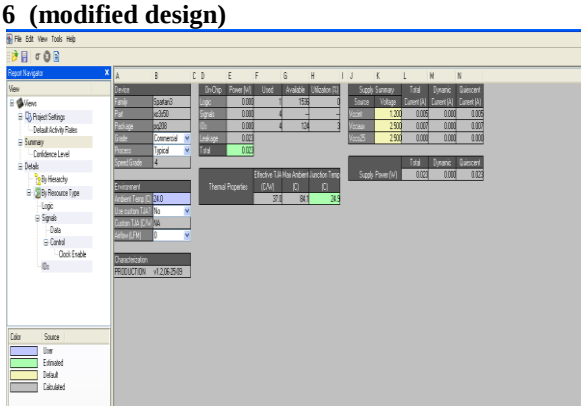

Figure 13. Power result of SRAM in SPARTAN 3e

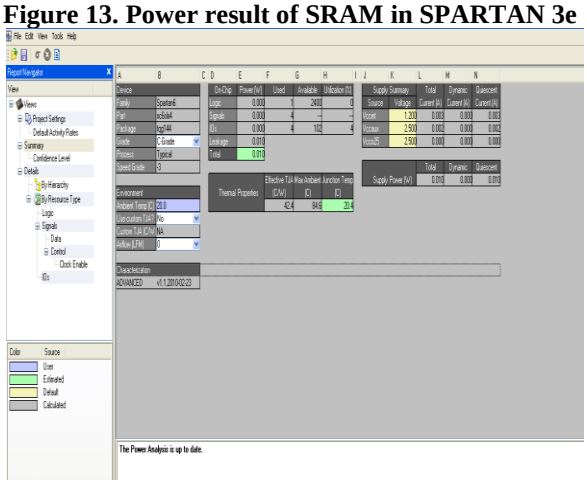

Figure 14. Power result of SRAM in SPARTAN 6

From the analysis, the power consumption of the existing dual V_{DD} is 0.029W which has to be verified via SPARTAN 3e family and the same has to be analyzed for SPARTAN 6 which gives the power output 0.011W. In this analysis report the switching activity of the capacitor is not to the extent to change the behavior of the dynamic current. Power estimation has to be analyzed based on the transistor activity and it is observed based on vector-less analysis.

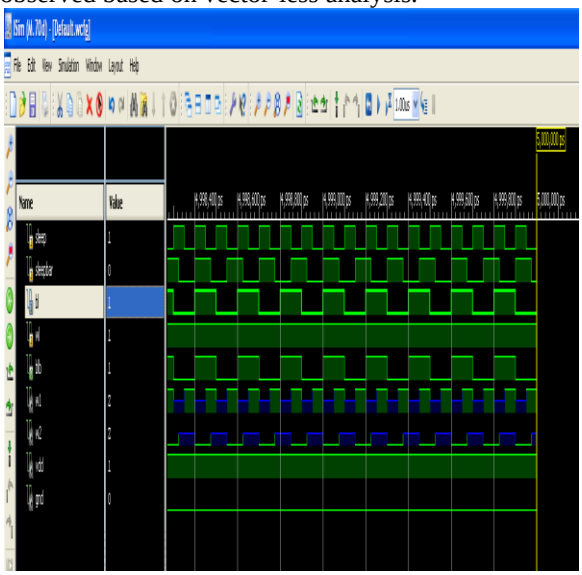

Figure 15. Simulation result of SRAM

As per the Transistor design of SRAM, wl and bl are the inputs which terms to be word line and bit line of the SRAM design which produce the output at blb based on the bit value.

3.3 Power result of FPGA in Spartan 3e, Spartan 6 (modified design)

Figure 16 and Figure 17 illustrates the power result of FPGA in SPARTAN 3e,6 family for the modified design. The dynamic power dissipation for the modified design is less than the dynamic power dissipation of the base design. From the analysis, the power consumption of the existing dual V_{DD} is 0.024W which has to be verified via SPARTAN 3e family and the same has to be analyzed for SPARTAN 6 which gives the power output 0.011W. In this analysis report, the switching activity of the capacitor is not to the extent to change the behavior of the dynamic current. Power estimation has to be analyzed based on the transistor activity and it is observed based on vector-less analysis. The power results show reduced leakage power for both Spartan 3e and Spartan 6 family for the modified design compared to the power results of Spartan 3e and Spartan 6 family for the modified design. The power results are obtained using Xilinx (Verilog) and the simulation result of SRAM is obtained using Modelsim.Hence power optimization is achieved.

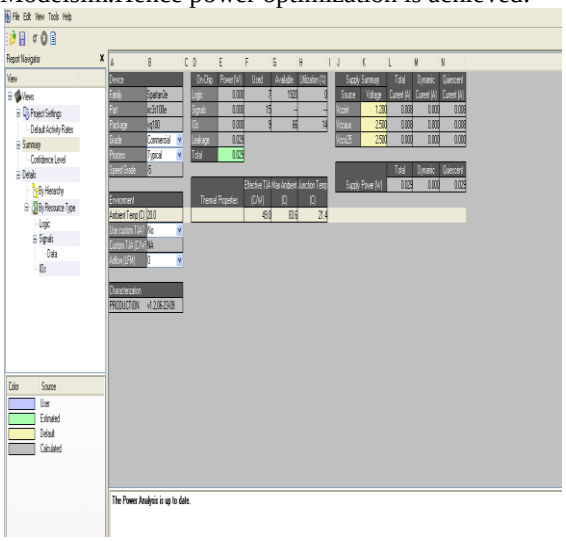

Figure 16 . Power result of FPGA in SPARTAN 3e

We analyzed the power consumed by SRAM and also the power consumed by FPGA which is illustrated in the power results in the manuscript. The major contribution of our work is in SRAM only which is used for FPGA applications.

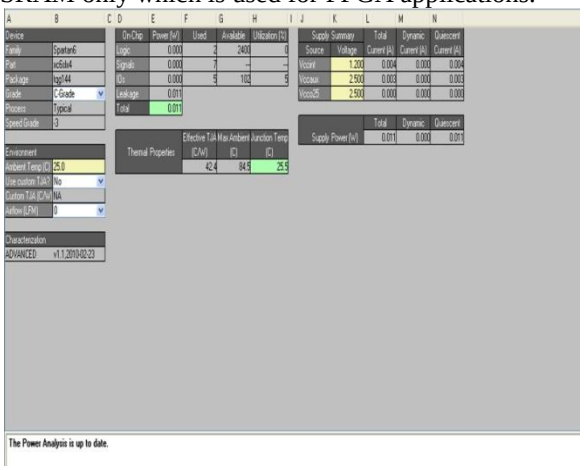

Figure 17 . Power result of FPGA in SPARTAN 6

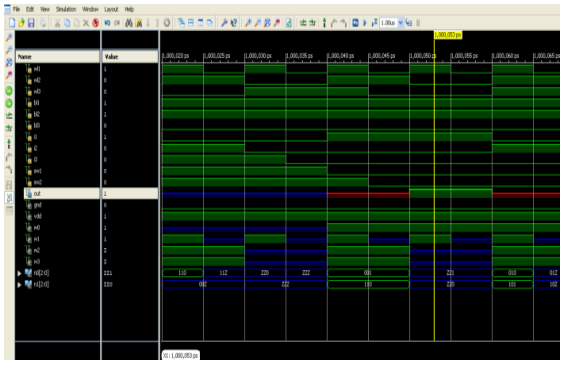

Figure 18. Simulation result of FPGA

As per the FPGA design, wl and bl are the inputs which terms to be word line and bit line of the FPGA design and sw1,sw2 are the switches which corresponds to V_{dd}-low and V_{dd}-high which produce the output at w based on the multiplexer configuration (select line).

3.4 Parameter Analysis for FPGA

Table 6 shows the power result comparison of Xilinx Spartan 3e family and Spartan 6 family for both the basic and modified designs. The leakage power in the modified design is 0.024 W which is less than the leakage power 0.030 W in the basic design for Spartan 3e family. Similarly, the leakage power in the modified design is 0.011 W which is less than the leakage power 0.015 W in the basic design for Spartan 6 family.

Table 6. Leakage Power reduction results of Spartan 3e family and Spartan 6 family (Base and modified design)

Circuit	Leakage power in Spartan 3e family (Watts)	Leakage power in Spartan 6 family(Watts)
Base	0.030W	0.015W
Modified	0.024W	0.011W

4. Conclusion

The noteworthy feature of FPGA design is based on the static and dynamic power dissipation. The reconfigurable design is proposed by changing the transistor design in the pull up network of the switching circuit. The proposed design gives less power and area than the traditional methods. The output shows the extensive amount of power reduction in V_{DDL} and $V_{DDH.}$ The simulation results are obtained using Verilog and Modelsim. This design plays its foremost contribution in current marketable FPGAs.

Acknowledgment:

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