An Hightened Switching Technique For An Interleaved Boost Converter Operated In Lower Duty Cycle

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Abstract: Interleaving technique in the boost converter effectively reduces the ripple current as a function of duty cycle. In this paper an improved switching technique for an interleaved boost converter is proposed and it is specifically designed for the converter operating under less than 50% duty cycle. In this technique, the auxiliary circuit resonance is composed of an inductor and a capacitor forming a resonant tank, which is used as controlling module as well as energy storage device for driving huge load even under lower duty cycle. An enhanced switching time of the converter is obtained due to the controlled resonance that decreases the number of phases of switching sequences. Inductor coupling in boost stages enables higher current sharing. In this topology, the time for attaining Zero voltage switching and zero current switching is greatly reduced due to the pre-excitation in main switches. The clamped diode acts as a bypass path that can reduce the loss in conduction. The design analysis is simulated using "MATLAB Simulink model" which illustrates the better performance of the converter.
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INTRODUCTION

Interleaving technique meritoriously increases the switching frequency without increasing the switching losses, thereby increase in the power density without compromising efficiency [1]. An interleaved topology improves converter performance at the cost of additional inductor, power switching devices, and output rectifiers [2]. Interleaving reduces the output capacitor ripple current as a function of duty cycle. As the duty cycle approaches 0 percent, 50 percent and 100 percent duty cycle, the sum of the two diode currents approaches dc. At these points, the output capacitor only has to filter the inductor ripple current [3]. The conventional boost converter is not suitable for the practical devices that produce low voltage levels, requiring large step up voltage and also to obtain such high gain [4].

Hence the lower duty cycle interleaved boost converters can be effectively used in the above application. Lot of research works in related to Zero-Voltage Switching (ZVS) and/or Zero-Current Switching (ZCS) have been analysed in the recent years. The main focus of the above is to reduce the switching loss of the high-frequency switching, and thereby, to obtain reasonable input current ripple, better switching time and overall efficiency. But these suffer from the following drawbacks,

1. The circuits proposed require complex auxiliary circuits to reach the smooth soft switching [5,6].
2. The main switches are ZCS and the auxiliary switches are ZVS during the whole switching transition while the auxiliary unit is complex due to extra inductor [5].
3. The main switches are ZCS at the turn-on transition, while in turn off the switching is hard [7].
4. The converter works in discontinuous mode with only limited duty cycle and with minimum load [8].
5. The number of switching phases and switching timing is high due to increased auxiliary resonance and voltage stress to the auxiliary switch [9].

In this paper an improved switching technique for an interleaved boost converter is proposed and it is specifically designed for the converter operating under less than 50% duty cycle. In this technique, the auxiliary circuit resonance is composed of an inductor and a capacitor forming a resonant tank, which is used as controlling module as well as energy storage device for driving huge load even under lower duty cycle. An enhanced switching time of the converter is obtained due to the controlled resonance that decreases the number of phases of switching sequences. Inductor coupling in boost phases enables higher current sharing. In this topology, the time for attaining Zero voltage switching and zero current switching is greatly reduced due to the pre-excitation in main switches. The auxiliary circuit reactance is further reduced which has decreased conduction loss in the converter. The clamped diode acts as a bypass path that can reduce the loss in conduction. Coupling capacity between auxiliary unit and main switch reduce the voltage stress over the switches during switching.

DESIGN AND ANALYSIS

For the case analysis, the circuit is analysed in continuous conduction mode (CCM) with various load ranges having different duty cycle. The Proposed interleaved Boost Converter with LC coupled Soft Switching is shown in Figure1. It utilizes the interleaved boost converter topology and applies enhanced soft switching methodology where the resonant tank itself triggers the switches for extreme condition. The resonant tank is composed of Resonant Capacitor C_{rc} and Resonant Inductor L_{rc} which in-turn act as a control circuit for the auxiliary switch S_{ax}, that is responsible for ZVS and ZCS function.

Principle of operation: The circuit is operated in fundamental mode with duty cycle D which is exact symmetrical in function. The circuit is analysed with certain assumptions to simplify the circuit analysis which are listed as,

- All switches and diodes are assumed to be in practical condition with an exponential decay α in the computation for theoretical analysis.
- Idealizing the input and output reactance.
- The two boost inductors are coupled.
- Same duty cycles (D_1=D_2) for the main switches S_{s1} and S_{s2}.

The flow of current in initial phases through the boost inductor has an effect of interference which results in addition of ripples. Thus, for the initial input current to be clear from input ripple, a guard is introduced, which is a magnetic couple by a ferrite core which has high permittivity and hence the coupling is more effective.

Boost inductors B_{L1} and B_{L2} is energized by the magnetic flow across the inductor causing fluctuation in the input current. It is minimized by placing the iron core between the coils which looks like a transformer arrangement. Thus the flow of current is regulated by the magnetic coupling across the inductors.

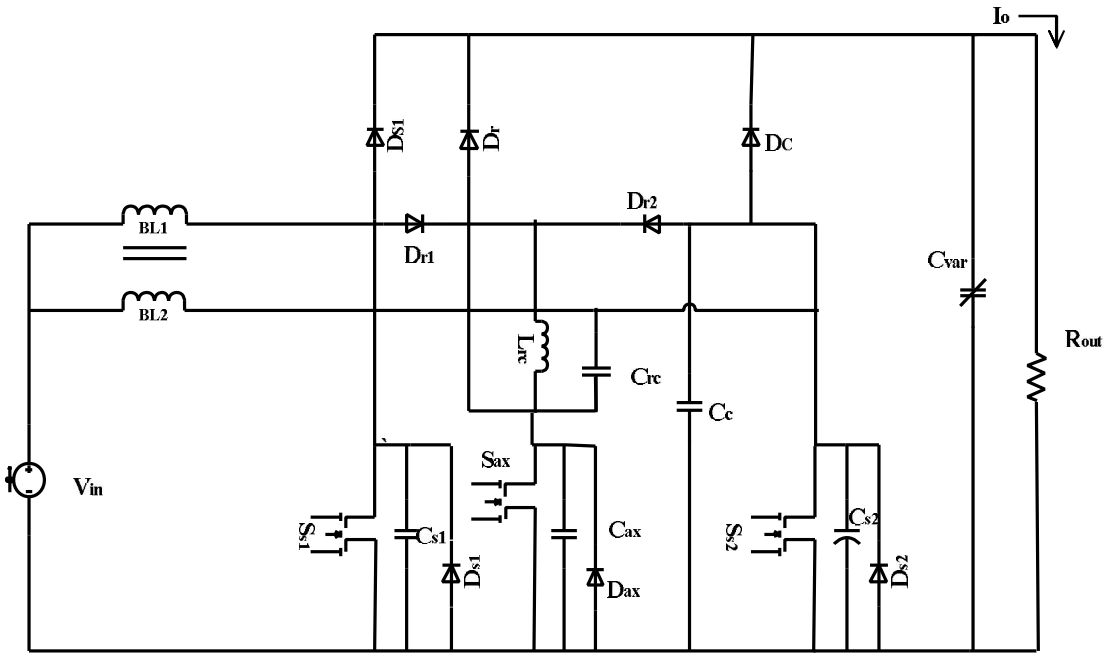


Figure 1. Proposed LC Resonant tank interleaved Boost Converter.

The mutual inductance exerted by both the boost inductor is given by,

$$L_m = \left(\mu_r \sqrt{L_1 L_2}\right) K \quad \ldots(1)$$

Where, μ_r & K are Permittivity of the core and coupling co-efficient respectively.

According to the circuit theory, the coupled inductor can be realized with an uncoupled inductor which needs an additional inductor for coupling. Thereby,

$$L_1' = L_1 - L_m \quad (2)$$

$$L_2' = L_2 - L_m \quad \ldots(3)$$

Where L_2' & L_1' are considered to be leakage inductances which has major influence over the input current ripple. By regulating the coupling coefficient, the amount of ripples in the input current can be controlled. On the other hand, the output from the inductor is given by the expression which depends only on the leakage inductance.

$$\frac{d_i L_1}{dt} = \frac{-V_0}{L_1' + L_m} = \frac{V_o}{L_1} \quad \ldots(4)$$

$$\frac{d_i L_2}{dt} = \frac{-V_0}{L_1' + L_2'} \quad \ldots(5)$$

The overall current in the converter is given by the equation (6), which is the hypotenuses cosine function of the capacitance.

$$I = \int_0^{t_6} -K\left(1 - \cosh\left[\frac{C_r + C_{sh}}{C_{sh} + C_r}\right]\right) dt \quad \ldots(6)$$

The significance of the equation is that overall effectiveness of current sharing of the converter is predetermined from the inductor current. Flow of current through the two switches is calculated by the following expressions (7) and (8).

$$I_1 = \sum_{S_{s1}=ON} \frac{V_{in}(1 - D_1 + D_{r2} + 2D_{rc})T}{L_1 L_2} \quad \ldots(7)$$

$$I_2 = \sum_{S_{s2}=ON} \frac{V_{in}}{1 - (D_r + D_{rc} + 2D_{rv})} \quad (8)$$

The overall cycle time is of the inductor output current with or without ripple and it can be expressed in the time of propagation of current in inductor, which is usually specified as a function of line frequency of input (i.e. Indian standards, 50 Hz).

$$T_{Cycle} = 2.37 \log_2 t_p \quad \ldots(9)$$

In this consideration of the switch S_{s1}, the total power applied to the auxiliary switch is given by the expression (10). The resistance in the parasitic (R) elements contributes for the maximum power usage in the switch.

$$P_{S1} = 2(I(t_p))^2 R \quad \ldots(10)$$

$$I(t_p) = \int_0^{tr} I_l(t) dt \quad \ldots(11)$$

$$I(t_p) = \int_0^{t_r} \left[-V_o \sqrt{\frac{C_1 C_s}{L_r(C + C_c)}} \sinh \sqrt{\frac{C_r + C_{ax}}{L_r C_1 C_{ax}}} + \frac{I_{L2} C_{ax}}{C_1 C_{ax}} 1 + \cos\left(\frac{C_1 + C_r}{C_1 C_r}\right) t \right] dt \quad \ldots(12)$$

The overall output current $I(t_p)$ in the converter is calculated as the integral of inductor current. The current purely depends on the resonant circuit of the device in use.

It is an inevitable fact that, in practical conditions, it is not possible to produce the duty cycle exactly at 50%., hence the design is analysed in duty cycle (D) lesser than 50%.

Operational analysis

Amidst 16 operational nodes in one complete cycle, only 8 nodes related with main switch S_{s1} are analysed and corresponding analytical equations are derived. The operating modes of the circuit for duty cycle less than 50% is shown in Figure 2 and Figure 3 shows the related wave forms under same condition. Figure 4 (a-h) shows the active phases of the converter during this duty cycle operation.

Phase I $[t_0 - t_1]$

In this phase, the initial voltage applied to the switch tends to vary due to the magnetic coupling in the inductor. Now the diode D_{r1}, D_{s1} becomes active, which act as a rectifier diode. The clamped diode D_r is turned off by the positive input cycle. At this juncture, the controls of switches are excited by pulse which is meant to turn off the switch S_{s1}, S_{s2}. Hence the parasitic capacitance C_{s1}, C_{s2} attached with the main switches and coupling capacitance share equal voltage. So it is given that $V_{c1} = V_{c2} = V_{cc} = V_0$ as the closed loop have equal voltage. Thus at the end time, the resonant inductor share the voltage applied across the circuit and the rectifier diode gets turned off. Under these circumstances the time interval can be calculated as

$$t_{01} = L_{B1}\left[\frac{V_0}{I_{Lin}}\right]^{-1} = L_{B1}\left[\frac{I_{Lin}}{V_0}\right] \quad (13)$$

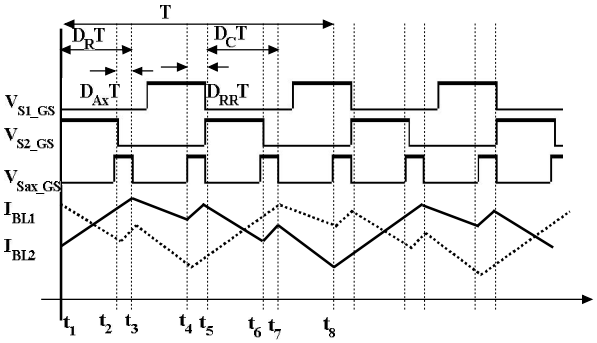


Figure 2. Driving Signal of the switches

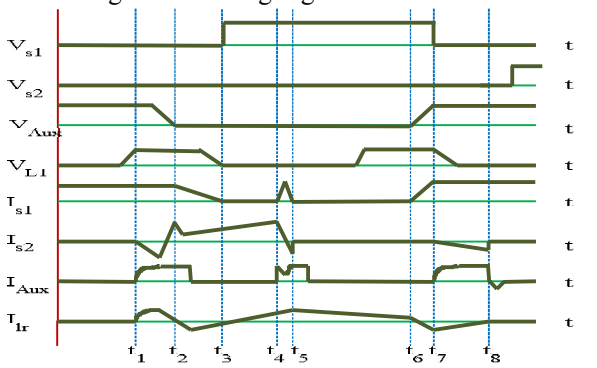


Figure 3. Switching phases

Phase II $[t_1 - t_2]$

In this phase, the resonant inductor tends to gradually increase to the peak value and the main switch gets reduced to lower values and becomes to zero. As a known consequence, the resonance occurs among C_{s1}, C_{s2}, C_c *and* L_{rc} .The diode in the switch bodies acts to turn on. Thus the resonant time t_{12} and the resonant inductor current $i_{L1}(t_2)$ is noted as,

$$t_{12} = \frac{\pi}{2\omega_1} = \frac{\pi}{2}\sqrt{L_{rc}(C_{s1} + C_{s2} + C_c)} \quad (14)$$

Resonant inductor current at the inductor L_v is given as,

$$i_{L_{rc}}(t_2) = I_{Lin} + \frac{V_0}{Z_0} = I_{Lin} + \frac{V_0}{Total\ impedance} \quad (15)$$

$$Total\ impedanc(Z_0) = \frac{1}{\sqrt{L_{rc}/C_{sh} + C_{s2} + C_{rc} + C_c}} \quad (16)$$

$$\omega_1 = \frac{1}{\sqrt{L_{rc}[C_{s1} + C_{s2} + C_c]}} \quad (17)$$

In this mode the resonant circuit gives additional control to the driving circuit which helps in reduction of switching phases of the converter.

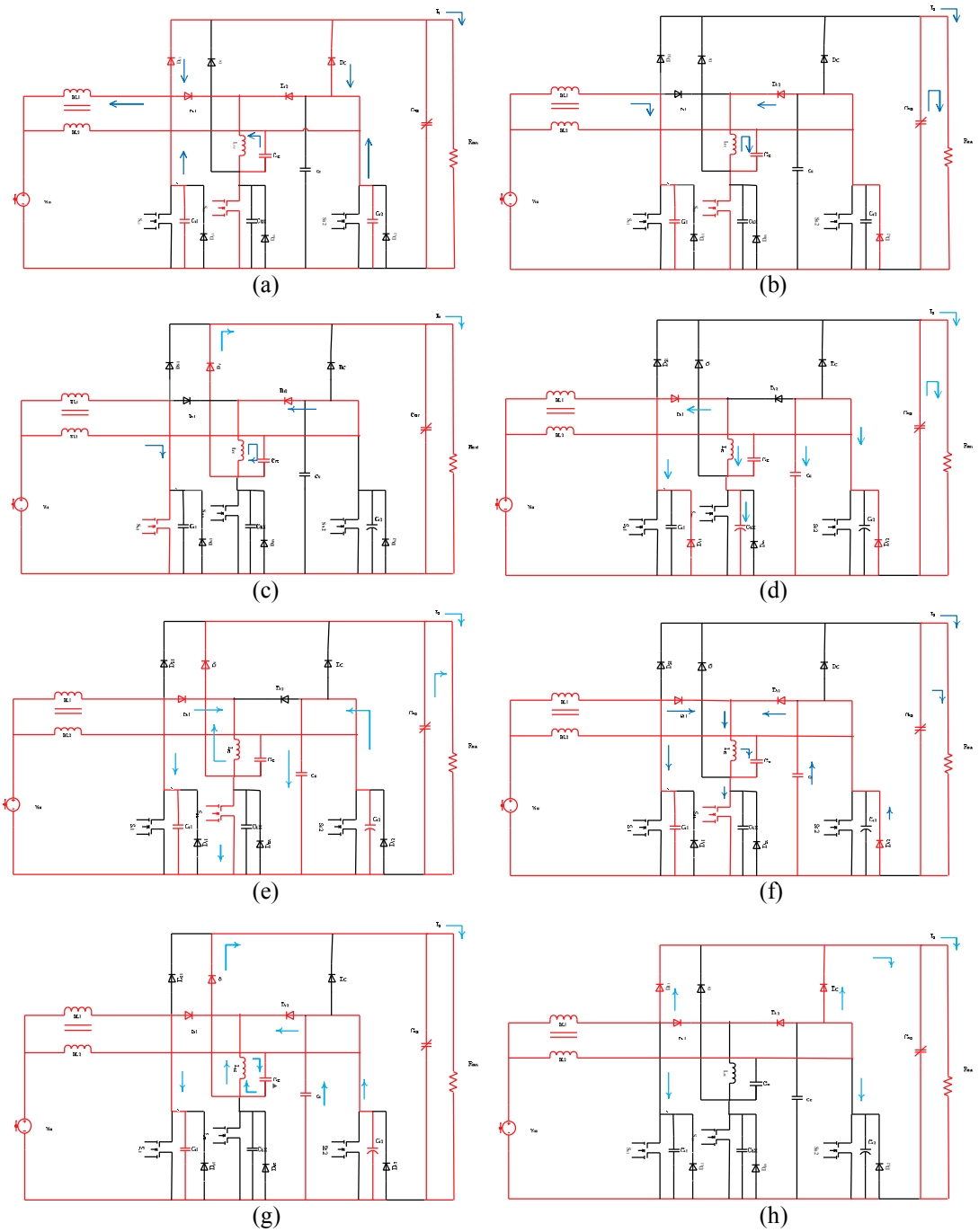


Figure 4. Operating modules when the duty cycle is less than 50% (a) Phase I (t0-t1) ,(b) Phase II (t1-t2), (c) Phase III (t2-t3), (d) Phase IV (t3-t4), (e) Phase V (t4-t5), (f) Phase VI (t5-t6), (g) Phase VII (t6-t7), (h) Phase VIII (t7-t8)

Phase III $[t_2 - t_3]$

At the end of Phase 2, the main switch voltage V_{s1} decrease to zero. So the diode of switch S_{s1} is turned ON at the end of t_2. In this phase, the main switch has the ability to achieve ZVS, the starting of t_{03} of the auxiliary switch S_{ax} needs additional time to achieve ZVS due to the presence of resonance in series. The maximum time is

$$t_{03} \geq t_{01} + t_{12} \quad \ldots(18)$$

$$t_{03} \geq L_{BL1}\frac{I_{Lin}}{V_0} + \frac{\pi}{2} I_{Lin}\sqrt{L_{rc}[C_{s1} + C_{s2} + C_c]} \ldots(19)$$

$t_{03} = t_{34}$, when D_r tends to turn ON. The current I_{Lin} & I_i are equal to

$$t_{34} = \frac{V_0}{V_{in}}\left[L_{BL1} + \frac{I_{Lin}(V_0)}{\sqrt{L_{rc}[C_{s1}+C_{s2}+C_0]}}\right] \quad \ldots(20)$$

Phase IV $[\boldsymbol{t_3 - t_4}]$

In this phase, the clamp diode D_r is turned off. Here the boost inductor (B_{L2}) charge is transferred to the C_c &C_{rc} coupling capacitor and resonant capacitor. The applied boost current to the capacitor energies the parasitic capacitors at C_{s2}& C_{ax} of the auxiliary switch and is transferred to the resonant inductor at the $I(t_r)$ which is given as, at $t_r = t_5$

$$I_{L_{rc}}(t) = \int_0^t \left[\begin{matrix} -v\sqrt{\frac{C_{s1}C_{sr}}{L_{rc}(C+C_{ax})}}\,sinh\sqrt{\frac{C_{rc}+C_{ax}}{L_{rc}C_{s1}C_{ax}}} + \\ \left\{\frac{I_{L2}C_{sr}}{C_{s1}C_{sr}} + C_{ax}\left(\frac{C_{s1}+C_{rc}}{C_{s1}C_{rc}}\right)\right\} \end{matrix}\right] dt \quad \ldots(21)$$

By simplifying,

$$I_{Lrc}(t) = \left[\begin{matrix} V_0\sqrt{\frac{CC_{ax}}{L_{rc}(C+C_{ax})}}\,sinh\sqrt{\frac{C_{s2}C_{sr}}{L_{rc}C_{s1}C_{sr}}} + \\ V_0\sqrt{\frac{C_{rc}C_{sr}}{L_{rc}(C+C_c)}} \end{matrix}\right] \quad \ldots(22)$$

Here

$$C = C_{rc} + C_c \& C_{sr} = \frac{C_{rc}C_{ax}}{C_{rc}+C_{ax}} \quad \ldots(23)$$

Phase V $[\boldsymbol{t_4 - t_5}]$

In this phase , the clamp diode D_r is excited to ON state. Thus the energy in the resonant circuit starts to discharge. The energy is transferred to output load via clamped diode $D_r$and it is turned on when the auxiliary switch S_{ax} is turned ON by the control from resonant circuit to the auxiliary circuit. Thus the time gap between the two phase s 4 & 5 is given by

$$t_{45} = D_I t_4 - [D_{rc}t_7 + t_{24}] \quad \ldots(24)$$

where,D_{rc} is duty cycle of Resonant Tank.

$$i_{Lrc}(t_5) \approx I_{Lrc}(t_4) \quad \ldots(25)$$

$$i_{Lrc}(t_5) = \left[\begin{matrix} V_0\sqrt{\frac{CC_{ax}}{L_{rc}(C+C_{ax})}} \\ \sinh\sqrt{\frac{C_{rc}C_{sr}}{L_{rc}C_1C_{sr}}} \end{matrix}\right] \quad \ldots(26)$$

This can be simplified as$i_{Lrc}(t_5) = I_{BL2} - I_0$.

Here the resonance tends to increase linearly with time as the boost current helps the resonant circuit to produce sustained oscillation and by the help of clamp diode, a pulse train control is imparted to the auxiliary switch.

Phase VI $[\boldsymbol{t_5 - t_6}]$

In this phase , the resonant circuit current I_{rc} increases linearly until it reaches I_{BL2} and the rectifier diode current I_{D1}decrease to '0'. This state is called critical state where the rectified input to the switches is zero. So the switch S_{s1} tends achieve, ZCS. So the main switch exhibits ZCS at Phase 6, whereas at Phase 3 it exhibits ZVS.

$$t_{5\alpha} = L_{rc}\frac{I_0}{V_0} \quad \ldots(27)$$

So that the condition at

$$t_{\alpha 6} = \frac{\pi}{2\omega_1} = \frac{\pi}{2}\sqrt{L_{rc}(C_{s1}+C_{s2}+C_c)} \quad \ldots(28)$$

Here the time of transition in ZCS is equal to the time transition at ZVS. So the excitation current at the switches are given by

$$I_{Lrc}(t_6) \approx i_{Lrc}(t_5) = \left[i_{Lrc}(t_2) + \frac{V_0}{\sqrt{\frac{L_{rc}}{(C_{s1}+C_{rc})}}}\right] \geq I_{Lin} \quad \ldots(29)$$

Here the time of ZCS is longer than the Model Switch.

Phase VII $[\boldsymbol{t_6 - t_7}]$

In this phase, both main switch and auxiliary switch is turned OFF and the stored charge in RC network is discharged to the load via D_r which is a clamped diode act as a bypass for the current flow and the input current charges the parasitic capacitance.

$$t_5 - t_6 = \frac{L_{rc}}{V_0}\left(i_{Lrc}(t_\alpha) + \frac{V_0}{Z_0}\right) \quad \ldots(30)$$

$$= \frac{L_{rc}}{V_0}\left(i_{Lrc}(t_\alpha) + \frac{V_0}{\frac{L_{rc}}{(C_{s1}+C_{rc})}}\right) \quad \ldots(31)$$

At this Phase all the voltages are tends to equal.

$$V_{rc}(t_7) = V_{s1}(t_7) = V_{s2}(t_7) = V_{cc}(t_7) \quad \ldots(32)$$

$$= \left[\begin{matrix} \frac{1}{(C_{s1}+C_{s2}+C_{rc}+C_{cc})} * \\ \int_{t_6}^{t_7}\left(I_{Lin} + i_{Lrc}(t)\right)dt \end{matrix}\right] \quad (33)$$

Now at this end of this phase, the charged inductor helps the rectifier diode to turn ON.

Phase VIII $[\boldsymbol{t_7 - t_8}]$

In this phase, the ideal nature of operation of the interleaved boost converter is obtained which is similar to that of conventional converter operation. This is the final phase, from which the control is transferred to the main switch S_{S2}. So this time can be called as regressive regeneration time of the converter which is mainly constant for the delay in switching. The time should be a fraction of normal operational time of phases

$$t_8 = \frac{T}{2} - \frac{(t_{01}+t_{12}+t_{23})}{L_{rc}C}V_0 \quad \ldots(34)$$

The new time t_8 is simple by afraction of only 8% of a half cycle. It is the symmetrical Phase for next switch that is incorporated to the system.

Voltage ratio

Voltage ratio is the actual ratio of voltages in active and inactive phases of a switch. This cannot be calculated by direct voltage comparison, so it is derived from the Boost inductor output current. It is derived specifically for the calculation of effective utilization of voltage in various duty cycles which shows the implication of it.

Boost inductor current $i_{B_{L_1}}$when switch is active in duty cycle less than 50%, where active phases are (t_{12}, t_{34}, t_{56}).

$$\sum_{s_1=ON} i_{BL1} = \frac{V_{in}}{L_{BL1}}(t_{12} + t_{34} + t_{56}) \quad \ldots(35)$$

$$= \frac{V_{in}}{L_{BL1}}(D_1 + 0.5D_r + 2D_{rr})T \quad \ldots(36)$$

Boost inductor current $i_{B_{L_1}}$when switch is

inactive in duty cycle less than 50%, where active phases are $(t_{01}, t_{23}, t_{45}, t_{67})$.

$$\sum_{s_1=OFF} = \left[\frac{[V_{in}-V_{out}]}{L_{BL1}}\left(\begin{matrix} t_{01}+t_{23} \\ +t_{45}+t_{67}\end{matrix}\right)\right] \quad \ldots(37)$$

$$= \left[\left[\frac{V_{in}-V_{out}}{L_1'}\right]\left[\begin{matrix} 1- \\ (D_1+0.5D_r+2D_{rr})\end{matrix}\right]T\right] \quad \ldots(38)$$

Then the conversion voltage ratio is derived as,

$$\frac{V_{out}}{V_{in}} = 1 - \frac{L_1}{L_1'}\left[\frac{1}{(D_1+0.5D_r+2D_{rr})}\right] \quad \ldots(39)$$

SIMULATION DESIGN AND ANALYSIS

Converter Specification

The switching frequency $f_s = 50Hz$, the output voltage $V_o = 440V$, and the range of output power P_{out} are $200W - 800W$. The range of operating voltages $150V - 220V$.

Estimation of boost Inductors & output capacitor

To support wide range of load a variable capacitor is used to provide impedance matching between the levels. The range of output capacitance is $200 - 700\mu F$ most preferably above $400\mu F$. The boost inductors B_{L1} & B_{L2} are designed to operate in CCM. The design consideration of the parameters are given by Calculation of inductance - Duty cycle less than 50%,

$$B_{L1\,min} = \frac{(D_r+2D_{rc})[D_1-(D_r+2D_{rc})]^2 R_{max}}{f_s} \quad \ldots(40)$$

Where, $D_r = 10\mu s, D_{rc} = 3\mu s,$

$$D_1 = 24\mu s, R_{max} = 10k\Omega, f_s = 50Hz$$

$$B_{L1} = 23\mu H$$

Estimation of Resonant Capacitor and Coupling Capacitor

Resonant capacitor plays an important role in all aspects of switching, energy storage, impedance matching and load driving etc., so the design of resonant capacitor enhances the overall performance of the converter. The total reactance of the system is the sum of reactance from capacitor and inductor which is equal to the overallenergy stored in the system.

$$Q = X_L + \frac{1}{X_C} \quad \ldots(41)$$

where X_L & $\frac{1}{X_C}$ are reactance of inductor and capacitor respectively.

Consider the charge and equivalent energy charge per storage in resonant tank. The operating frequency of the tank circuit is given by 50Hz, so the calculation of resonant capacitor is obtained from (63) by substituting known values,

$$\frac{1}{f_s} = \frac{\pi}{2}\sqrt{L_r(C_{S1}+C_{S2}+C_c+C_r)} \quad \ldots(42)$$

By simplification with the known values of maximum allowed parasitic capacitance in MOSFET switches, the coupling capacitance and resonant capacitance is given as $1.5\mu F$ *and* $2.5\mu F$ respectively.

Design of Arrival Time of ZVS Condition

When time taken by the switch S_{S1} to achieve ZVS, the voltage across the source to drain must be zero. The same is achived in Phase 3 for mode D<50%. The minimum time considered for the arrival of ZVS is given by,

For Phase 3 (D<50%), the calculation of ZVS arrival time is given as,

$$D_{S1} > t_{23} = \frac{\pi\sqrt{L_{rc}(C_{S1}+C_{S2}+C_c+C_{rc}}}{2} \quad \ldots(43)$$

$$= \frac{3.14 \times \sqrt{5\mu \times 840p}}{2} = 203.50ns$$

Design of Arrival Time of ZCS Condition

Time at which the switch S_{S2} achieve ZCS is in Phase 5 for mode D<50%. The minimum time considered for the arrival of ZCS is given by the resonant inductor current.

Therefore in Phase 5 (D<50%), the calculation of ZCS arrival time is given as,

$$i_{Lrc}(t_5) = I_{BL2}(t_\alpha) + \frac{V_o}{Z_1} = 6.905A > I_{in} \quad \ldots(44)$$

$$D_{S1} > t_{4\alpha} + t_{\alpha 5} = L_{rc}\frac{I_o}{V_o} + \frac{\pi\sqrt{L_{rc}(C_{S2}+C_c+C_{rc})}}{2} \quad \ldots(45)$$

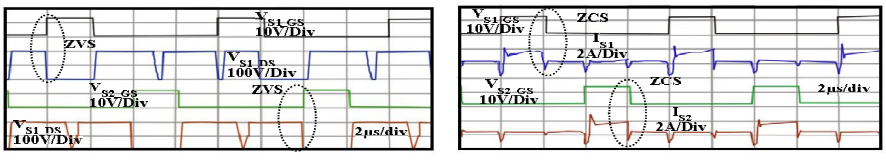
$$= 225ns$$

Thus, the design can give the Maximum Duty time of soft switching condition with the above constraints. All the above parameter values are tabulated in Table 1.

Table 1. Parameters and components of the converter

Input Voltage	180-240V
Duty Cycle	<50% for Simulation 25%
Output voltage	440V
Output Current	0.5A-1.45A
Output power	200-800W
Switching frequency	50Hz
Boost_L1 and Boost_L2	23µH, Ferrite core $\mu_r = 10$
Output capacitor	200-700µF
Resonant inductor	5µF
Resonant Capacitor	1.5pF
Coupling Capacitor	2.5pF

SIMULATION RESULTS AND DISCUSSIONS



(a) (b)

Figure 5. Simulation waveforms of the main switches S_{S1}, S_{S2} (a)(b) ZVS and ZCS operation while operating in duty cycle below 50% with load current 0.55A.

Above output shows the operation of the converter under the variation load from 200 to 800W with the duty cycle less than 50%.Based on the design consideration and required conditions, the proposed interleaved boost converter with both ZVS and ZCS characteristics is built and it is shown in concerned places with proper indication. The simulated output waveforms (Figure 5) of the proposed circuit are obtained with an input voltage of 150V and the load current of ~0.6A. While verifying the output of both the switches S_{S1} and S_{S2}, it will be same, as the circuit is symmetrical. The proposed method has a designed switch with a practical decay constant (α) which is dependent factor on temperature, working life span, range of conductivity, and various physical factors.

Various switching timings are tabulated in Table 2 which compares the switching timing of existing converters and proposed converter. The switching timing of the proposed converter indicates the fast switching transition of the circuit when compared with existing topologies. Further, the results shows that the proposed converter can be implemented with better power factor for the practical applications like Solar System, PV Panel, Grid Systems, Green Power System and Semiconductor Industries.

Table 2 – Comparison of Switching Timings

Switching Constraints	Enhanced Soft Switching with ZVS and ZCS	Soft Switching with ZVS and ZCS(2012)[9]
Time for ZCS Duty Cycle<50%	225ns	249ns
Time for ZVS Duty Cycle <50%	203.5ns	225ns

CONCLUSION

An improved soft switching technique for an interleaved boost converter operating under less than 50% duty cycle is proposed in this paper. The main switches S_{S1} and S_{S2} can achieve both ZVS and ZCS, which can also be adjusted by driving circuit through LC resonant. The sharing of input current is equal between the switches.It uses tank circuit composed of resonant inductor L_{rc} and resonant capacitor C_{rc} , parasitic capacitance in switches $C_{S1}$and C_{S2}, coupling capacitor C_c and an auxiliary switchS_{ax}, that provides a path to achieve ZVS and ZCS of the main Switches S_{S1} and S_{S2}.Ferrite Core and coupling capacitor $C_c$act as an efficient ripple filter to minimize input current ripple.The circuit can drive heavy load with greater efficiency due to impedance matching which is achieved by energy storing elements (resonant tank and variable output capacitor). Better switching timing for ZVS and ZCS is also obtained by using bypass networks. The number of phases has been reduced without affecting the smooth soft switching and revels the best.

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