

Design of a Reversible Ripple Carry Adder for Excess-3 Code

Vida Abdolzadeh¹, Nasser Lotfivand², Siamak Haghipour³

¹ Department of Computer Engineering, Tabriz Branch, Islamic Azad University, Tabriz, Iran

² Department of Electronic Engineering, Tabriz Branch, Islamic Azad University, Tabriz, Iran

³ Department of Biomedical Engineering, Tabriz Branch, Islamic Azad University, Tabriz, Iran

S.V.Abdolzadeh@iaut.ac.ir, Lotfivand@iaut.ac.ir, Haghipour1@yahoo.com

Abstract: One of the main characteristic in VLSI circuits is power dissipation. Due to the information loss, conventional logic circuits result in energy dissipation. Reversible circuits because they do not lose information, have zero internal power dissipation. This paper proposes a reversible 4-bit parallel adder for Excess-3 code. Excess-3 is an unweighted and self-complementing code. Excess-3 coding over BCD coding has various advantages. The primary superiority is that a decimal number can be nines' complemented (for subtraction) as facily as a binary number can be ones' complemented by inverting all bits. The proposed Excess-3 adder in the number of reversible gates and garbage outputs, allowing high-speed and low-power reversible circuits, covers all favorable characteristics of reversible circuits.

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1. Introduction

High growth rate in portable systems have caused requests for power-sensitive designs increase. As a result, new power-efficient design techniques have been considerable subject for researchers. In 1966, Landauer's researches demonstrated that the minimum energy dissipation for every irreversible bit operation is $kT \ln 2$ joules, where $k = 1.3806505 \times 10^{-23}$ is Boltzmann's constant, and T is the environment's temperature [1, 2]. Bennett found $kT \ln 2$ energy consumption can be avoided, when the system regenerates inputs base viewed outputs [3]. Recently, several technologies subsuming, low power CMOS technologies, optical technologies, quantum computing, DNA computing and nanotechnology for reversible logic have been studied [4].

In a reversible circuit each input is mapped to a singular output, and this mapping must be bijective. The number of inputs and outputs, in a reversible circuit, are the same. These circuits make possible inputs denominate from outputs [5, 6, and 7]. Fan-out or feedback in reversible logic is not allowed, so the synthesis of a reversible circuit is principally more hard set in contrast with conventional logic [8].

Excess-3 is an unweighted and self-complementing code. Excess-3 coding over BCD coding has various advantages. The primary superiority is that a decimal number can be nines' complemented (for subtraction) as facily as a binary number can be ones' complemented by inverting all bits [9]. In this paper, we propose an Excess-3 Adder design using reversible logic gates. The design is based on Feynman Gate and Haghparast--Navi gate.

The rest of the paper is organized as follows: Section 2.1 provides the basic concepts. Section 2.2 discusses the proposed circuits. Section 3 concludes our work.

2. Material and Methods

2.1 Basic Concepts

An α -input and β -output function $f: B^\alpha \rightarrow B^\beta$ is a reversible function if and only if:

- $\alpha = \beta$, where α and β are the number of inputs and outputs, and
- it maps each input to a unique output

With a cascade of reversible gates g_i we can synthesize a reversible circuit $G = g_0 g_1 \dots g_{k-1}$ over inputs $X = \{x_1, x_2, \dots, x_n\}$. We can represent a reversible gate with $g(C, T)$, where C contains the Control lines, and may be empty. T represents the Target lines. If and only if the control lines satisfy the control conditions; the gate operation is then applied to the target lines [10]. Many reversible gates exist, and we present some common reversible gates below:

Figure 1.a shows a 2*2 Feynman Gate, also known as 1-CONT [11]. Figure 1.b depicts a 3*3 Toffoli Gate [8]. The inputs 'A' and 'B' are passed as first and second outputs, respectively. The first and second inputs control the third output to invert the third input. Figure 1.c shows a 3*3 Peres Gate (PG) [12], also known as a New Toffoli Gate; a Peres gate combines a Toffoli and Feynman Gate. Figure 1.d shows a 3*3 Fredkin Gate [13]. Here, input 'A' is passed as the first output. Inputs 'B' and 'C' are swapped to obtain the second and third outputs, controlled by 'A'. If $A = 0$, the outputs are simply

duplicates of the inputs; otherwise, if $A = 1$, the two input lines (B and C) are swapped.

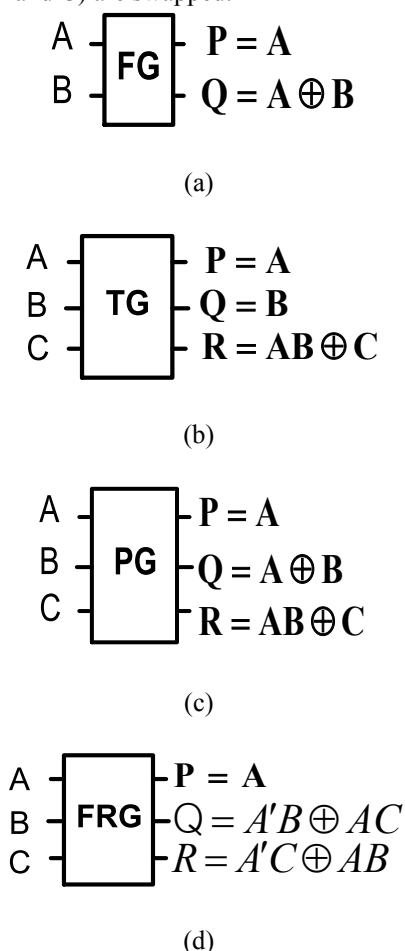


Figure 1: Commonly used reversible gates. a) Feynman gate; b) Toffoli gate; c) Peres Gate; d) Fredkin Gate

2.2 The proposed Reversible 4-bit Adder for Excess-3 codes

One of the widely used elements in digital circuits, are full adders. Researchers have introduced various designs for a reversible full adder [2, 4, 14, 15, 16], but to our knowledge, no research has presented a design for a reversible 4-bit parallel Excess-3 adder. Our design uses Haghparast-Navi gates (HNG) (as in [2]), which can work as a reversible full adder unit, shown in Figure 2.

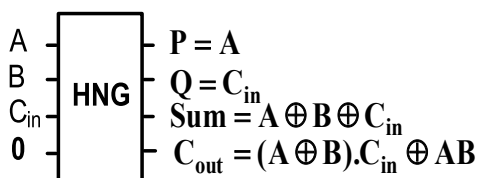


Figure 2: HNG gate as Reversible Full Adder

An Excess-3 adder circuit adds two Excess-3 numbers and converts the results into the equivalent Excess-3 number. Figure 3 illustrates the block diagram of the proposed Excess-3 adder. The circuit uses two 4-bit binary adders. The first adder's inputs are Excess-3 numbers, producing an excess-6 sum. Conversely, when the two decimal numbers sum to 9, the first adder's output is 15; if their sum is 10, the output of the first adder is 0, and the output carries a bit if the first adder goes high.

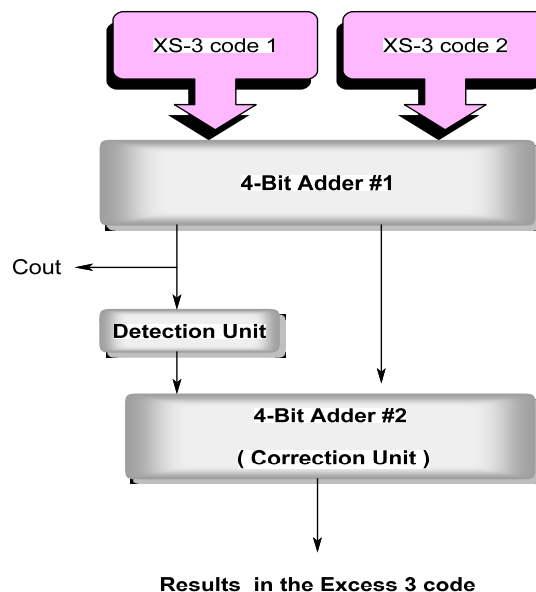


Figure 3: Block diagram of the proposed 4-bit Excess-3 adder

If and only if the two decimal digits' sum is greater than 9, $Cout=1$. These are the cases for which a carry must be activated. Achieving an Excess-3 sum in the circuit requires some correction in the first adder's output. The second adder performs this correction.

To convert an Excess-6 value to an Excess-3, if $Cout=0$ in the first adder, correction occurs by subtracting 3 from the sum of the first adder. If there is a carry, correction occurs by adding 3. When the two decimal numbers sum to 10, the output of the first adder is 0000, and $Cout=1$. By the second adder 3 is added to 0000 that creates 0011 in the result (the Excess-3 representation for 0).

If $Cout=0$, it subtracts 3 by adding 2s complement of 3. This subtraction occurs in two steps. It first adds the bit-wise complement of 0011 (e.g., 1100) to the output of the first adder and then adds 0001 to this result, by inputting 1 to the Cin of the second adder.

An implementation of proposed circuit by FPGA showed good performance of circuit. Figure 4 depict RTL schematic of the circuit and Figure 5 shows simulation results.

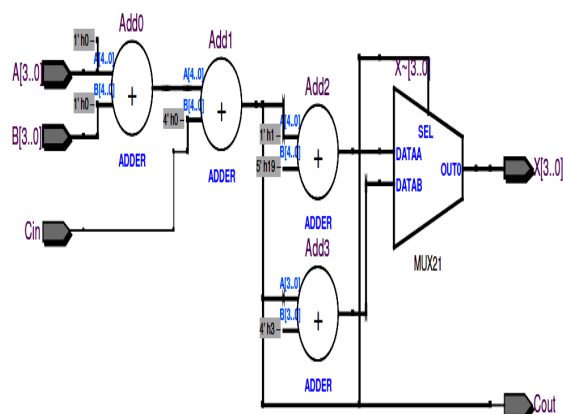


Figure 4: RTL schematic of implemented proposed adder by FPGA

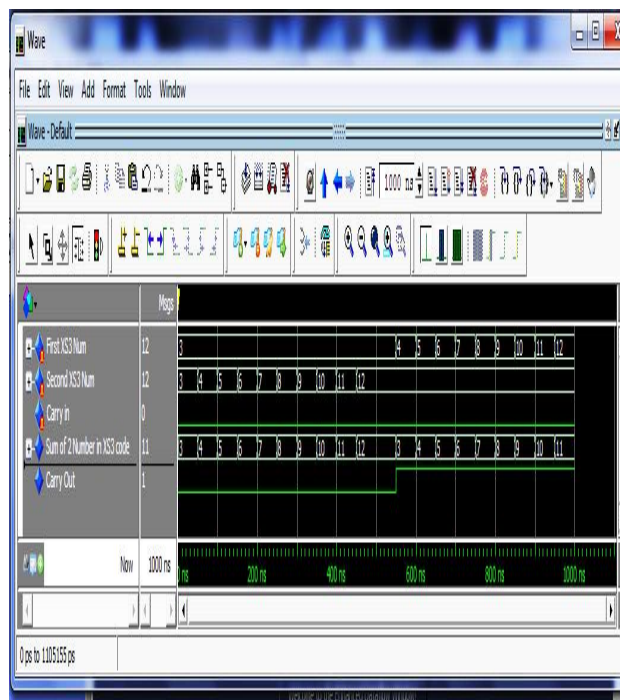


Figure 5: Simulation results

Figure 6 represents the proposed reversible 4-bit parallel Excess-3 adder using HNG gates. The proposed Excess-3 adder has two reversible 4-bit parallel adders implemented by eight HNG gates. It also requires five Feynman gates to avoid bit fan-out. Therefore, the total number of gates required to construct the reversible 4-bit Excess-3 adder is $2*4+5=13$.

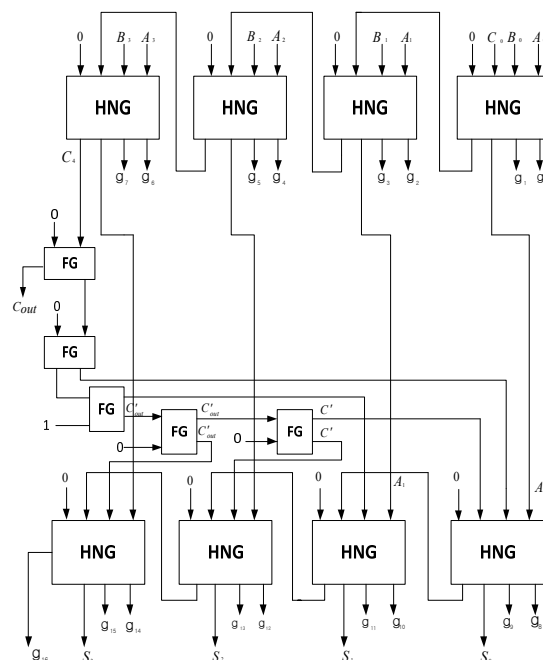


Figure 6: The proposed reversible 4-bit Adder for Excess-3 code

The proposed Excess-3 adder uses four reversible full adder circuits to construct a reversible 4-bit parallel adder; each full adder circuit produces two garbage outputs. The total number of garbage outputs generated from the 4-bit reversible adder is eight. The five Feynman Gates, which copy bits, do not produce any garbage outputs. The last carry in the second 4-bit adder is garbage. The total number of produced garbage outputs is thus $2*8+1=17$ (the circuit has two 4-bit parallel adders).

Hardware complexity is a major representative for a digital circuit's evaluation. With the four main factors of circuit complexity defines as: α is the number of two-input EX-OR gate, β is the number of two-input AND gate, δ is the number of NOT gate, and T is Total logical calculation. The total logical calculation of this circuit is $T=45\alpha + 16\beta$, and it uses only 13 gates. Decreasing of the number of garbage outputs is another definitive criterion in designing a reversible full adder. Garbage output is an output that is not input to other gates or is not a primary output. The purposed circuit in the hardware complexity, number of reversible gates and garbage outputs, demonstrates the good features of reversible circuits.

3. Conclusion

In this paper, we proposed a reversible 4-bit parallel Excess-3 adder by using HNG and FG gates. Table 1 shows features of this circuit.

Table 1: features of reversible 4-bit parallel Excess-3 adder

Number of Reversible Gates	13
Number of Garbage Outputs	17
Total Logical Calculation	$45\alpha + 16\beta$

For quantum computers and nanometric-based systems, a reversible arithmetic unit is a compulsory need. The proposed circuit can be utilized as a building block for synthesizing a reversible arithmetic unit.

The proposed Excess-3 adder in the number of reversible gates and garbage outputs, allowing high-speed and low-power reversible circuits, covers all favorable characteristics of reversible circuits.

Corresponding Author:

Nasser Lotfivand

Department of Electronic Engineering, Tabriz Branch, Islamic Azad University, Tabriz, Iran E-mail: Lotfivand@iaut.ac.ir

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